Reed Electronics Group

EDN

VOICE OF THE ENGINEER

MAY 15

Issue 10/2008

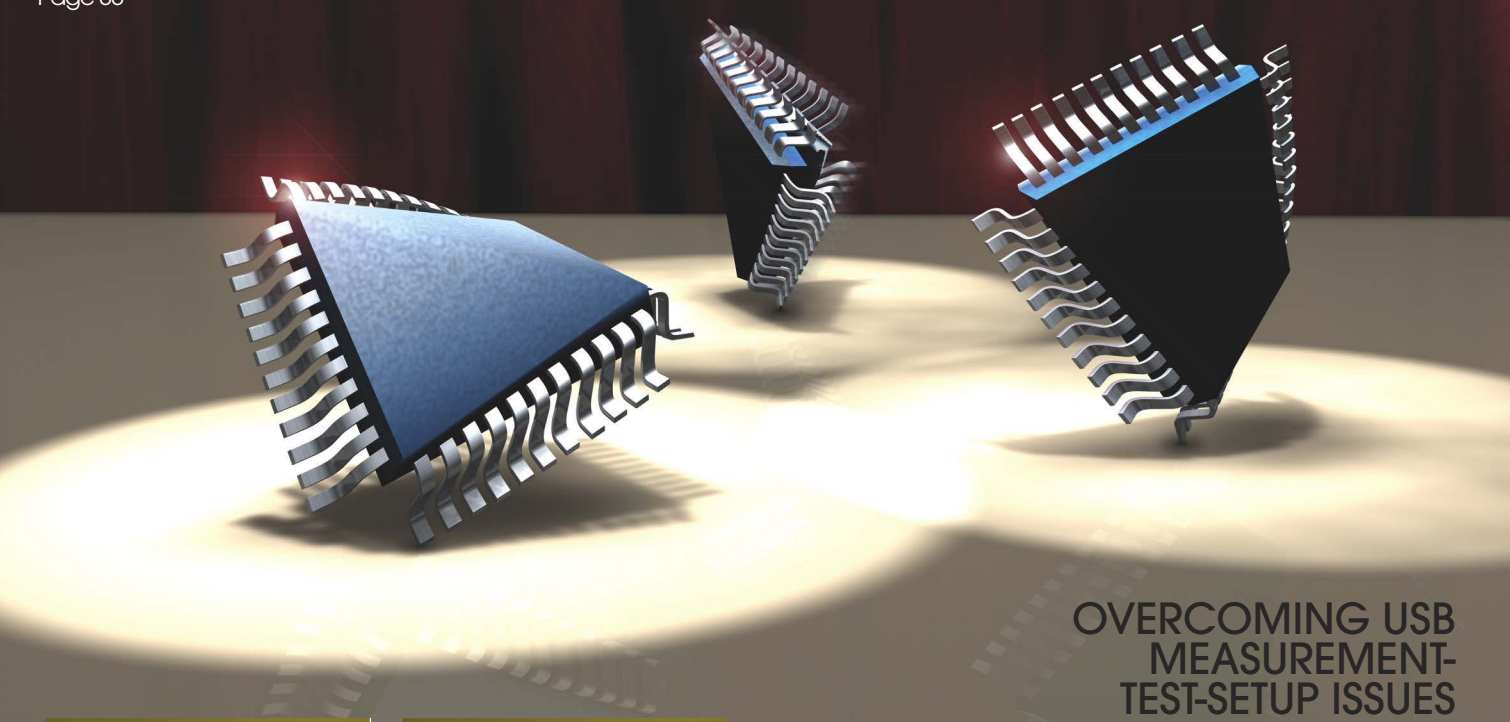
www.edn.com

FLEXIBLE SILICON

page 40

ALWAYS ON: EMBEDDING HIGH AVAILABILITY

Page 33



OVERCOMING USB MEASUREMENT-TEST-SETUP ISSUES

Page 49

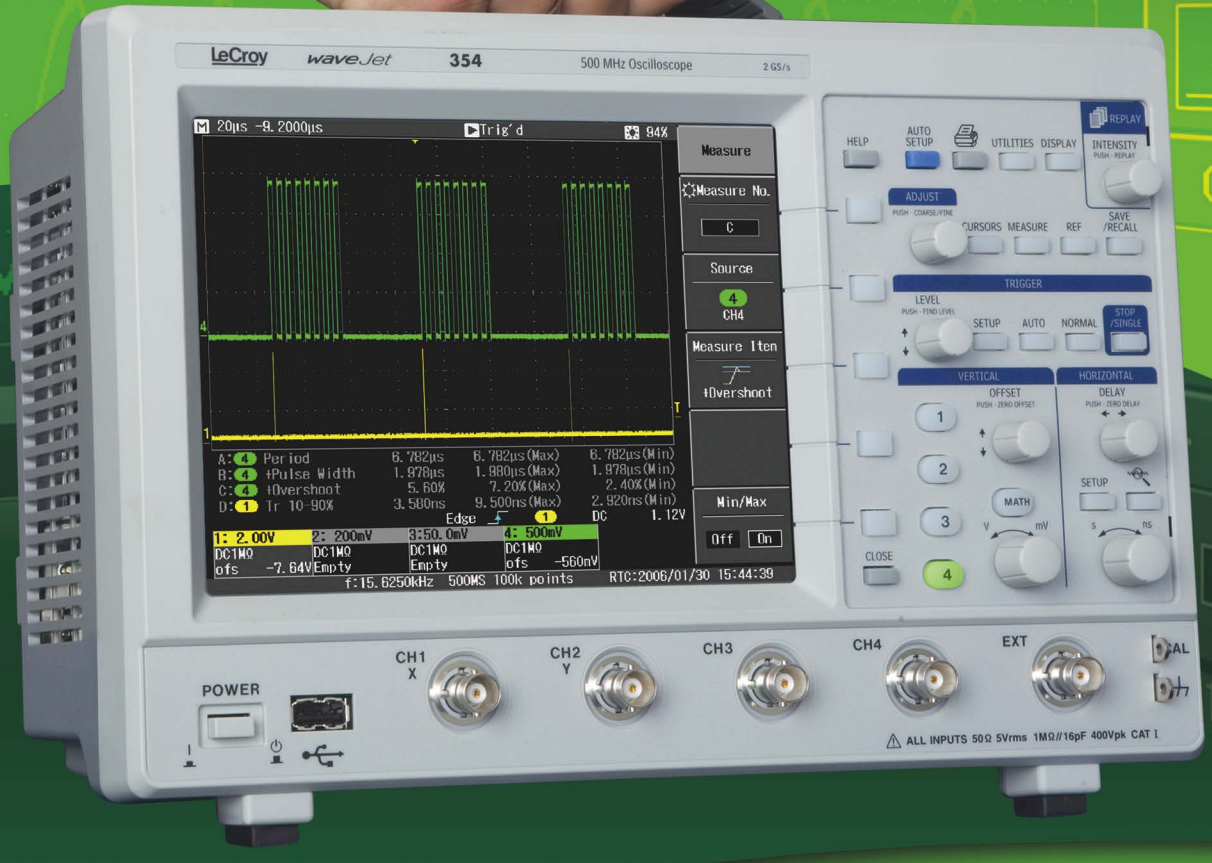
TESTING YOUR NOTEBOOK DESIGN FOR AUDIO FIDELITY

Page 55

All the right tools in your hand.

WaveJet® Oscilloscopes

FROM $2,950



More tools. Better tools. The right tools.

The right tools make debugging faster and easier. The WaveJet 300 Series provides more tools and greater performance than other compact oscilloscopes in the 100 MHz to 500 MHz range.

- *Long Memory: 500 k/ch*
- *Large 7.5" Color Display*
- *Compact Size, only 4" Deep*
- *USB Connectivity*
- *Replay History Mode*
- *Frequency Counter*

www.lecroy.com 1-800-5-LeCroy

LeCroy

SAME-DAY SHIPPING on orders entered by 8:00 pm CENTRAL
NEXT-DAY DELIVERY

Hundreds-of thousands* of parts in stock. Visit www.digikey.com today to see how many!

Quality Electronic Components, Superior Service

Digi-Key Corporation purchases all product directly from its original manufacturer.

www.digikey.com
1.800.344.4539

701 Brooks Ave. South • Thief River Falls, MN 56701 • USA

*New product added daily.

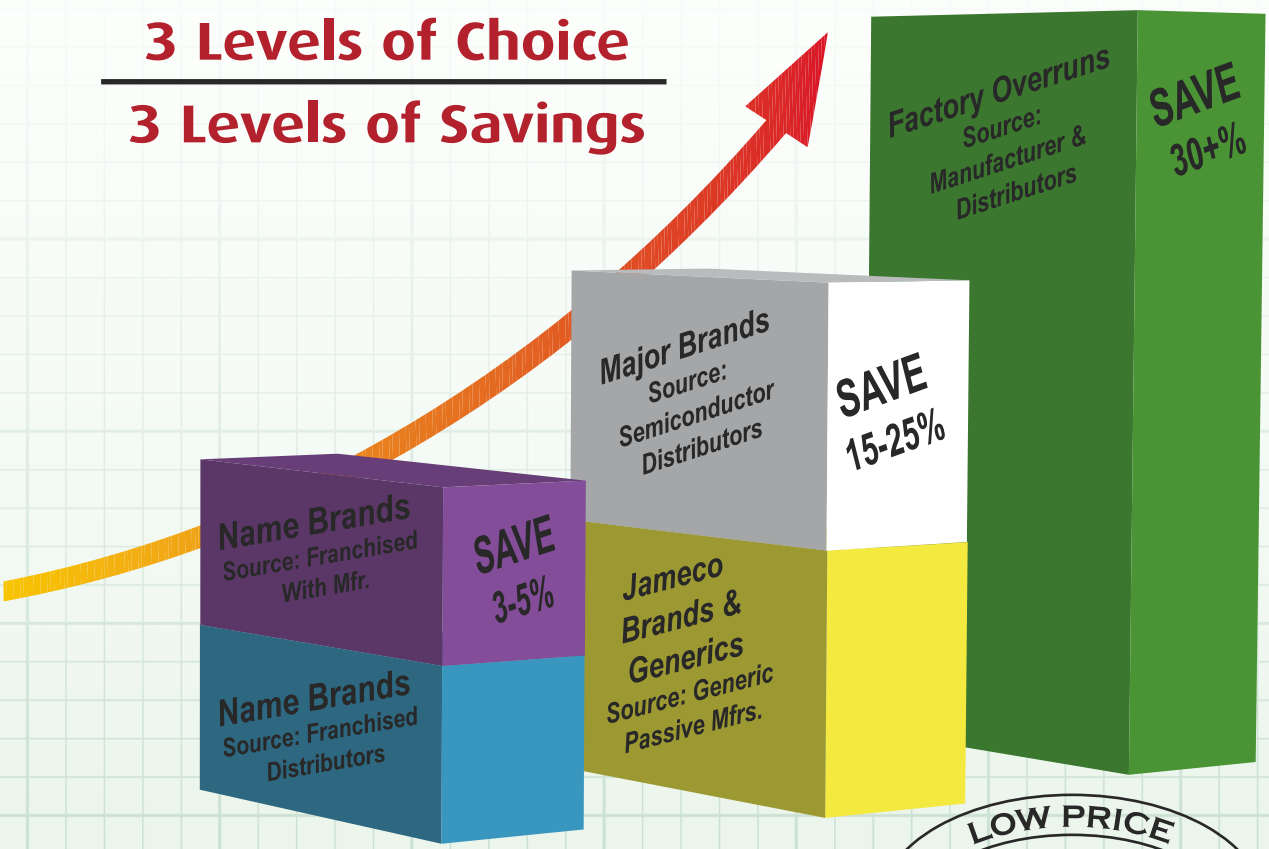
Exclusively at Jameco... The Lowest Prices... Guaranteed!

Save 3% to 5%
Looking to save on thousands of Name Brand components? Jameco offers their popular products for 3% to 5% below market price, and we guarantee it!

Save 15%-25%
Save more when a specific manufacturer is not required. Major Brand semi's are sourced from 5-6 major manufacturers, plus we offer Jameco brand and generic passives for even greater savings.

Save 30% or more!
Looking for killer deals? Jameco buyers often find Factory Overruns from some of the industry's biggest names. That means savings of 30% and more to you!

3 Levels of Choice
3 Levels of Savings



Other Jameco Advantages:

- We offer over 300 Major Manufacturers
- ***99%*** of catalog products ship the same day.
- Lowest prices guaranteed, or we pay 10%.

LOW PRICE GUARANTEE

If you find a lower print-advertised price for a product we offer, just let us know. We'll offer you that product for 10% less than the price you found, right down to our cost!

JAMECO® ELECTRONICS

Order 24 hours a day, 7 days a week

www.Jameco.com

Or call 800-831-4242 anytime

SEMICONDUCTORS • PASSIVES • INTERCONNECTS • ELECTROMECHANICAL • POWER

Enter the New World of Bourns

Automotive Sensors

Circuit Protection Solutions

Magnetic Products

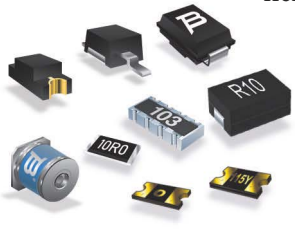
Microelectronic Modules

Panel Controls & Encoders

Precision Potentiometers

Resistive Products

The world of Bourns has grown. An expanding world focused on exceeding our customers' needs. New innovative products and technologies. Expanded application solutions. Plus a worldwide team of technical experts to facilitate the design process and solve tough application problems. All provided to help customers shorten design cycles and achieve faster time-to-market.



At Bourns, we have grown to serve you better. Step in – explore the new world of possibilities from Bourns today:

www.bourns.com/newworld

Bourns - *the company you have relied on for more than 60 years.*

BOURNS®

Built on Trust…Based on Innovation

Green Engineering

Powered by National Instruments

MEASURE IT

Acquire environmental data from thousands of sensors

Analyze power quality and consumption

Present measured data to adhere to regulations

FIX IT

Design and model more energy efficient machines

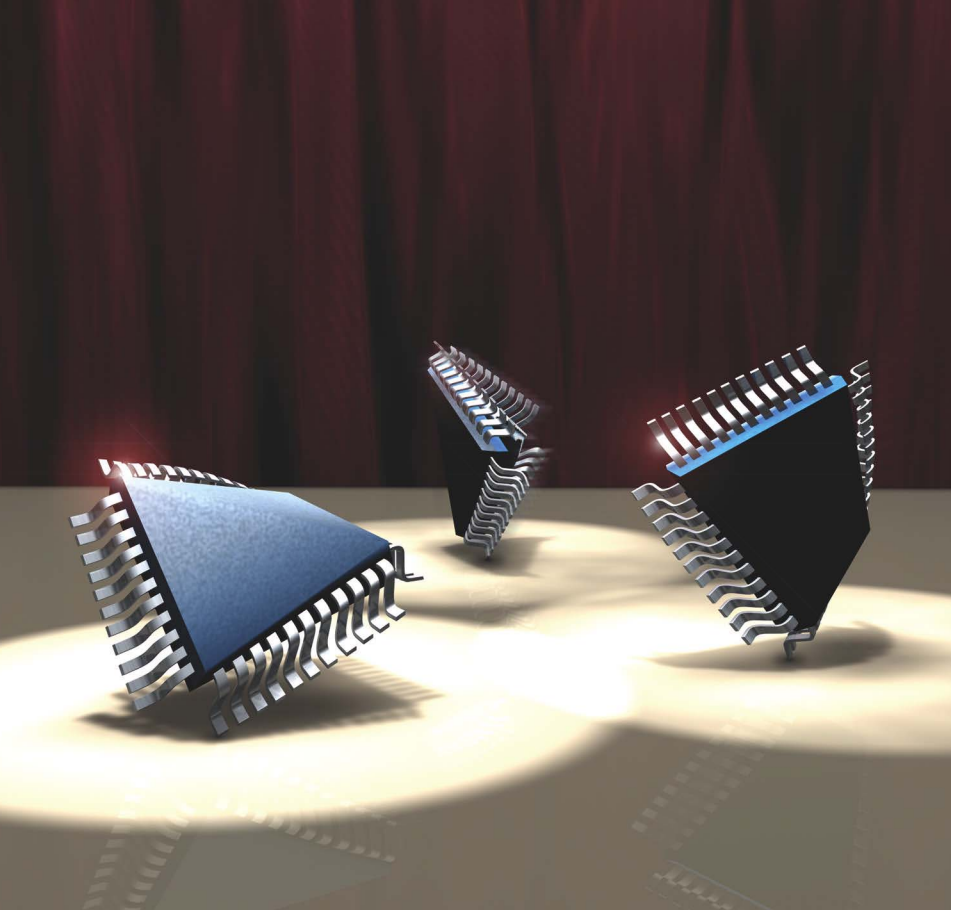
Prototype next-generation energy technologies

Deploy advanced controllers to optimize existing equipment

For more than 30 years, National Instruments has empowered engineers and scientists to measure, diagnose, and solve some of the world's most complex challenges. Now, through the NI graphical system design platform, engineers and scientists are using modular hardware and flexible software to not only test and measure but also fix inefficient products and processes by rapidly designing, prototyping, and deploying new machines, technologies, and methods. Today, a number of the world's most pressing issues are being addressed through green engineering applications powered by NI products.

>> Download green engineering resources at **ni.com/greenengineering** **800 890 1345**

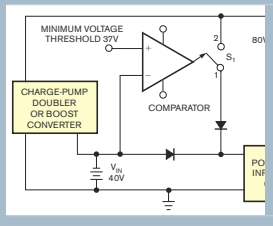
NATIONAL INSTRUMENTS™

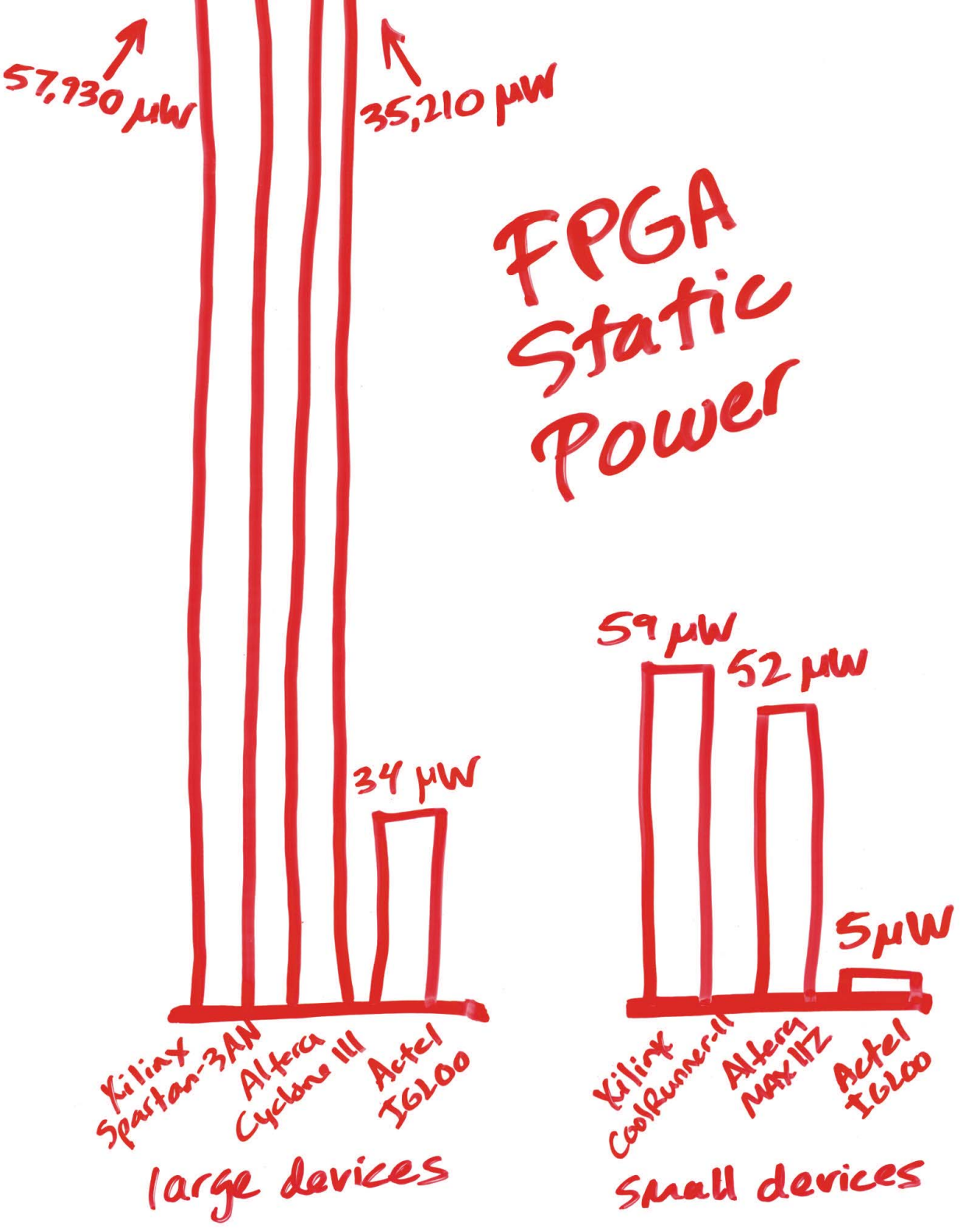


EDN contents

5.15.08

DESIGNIDEAS





WHAT DO WE HAVE TO DO, DRAW YOU A PICTURE?

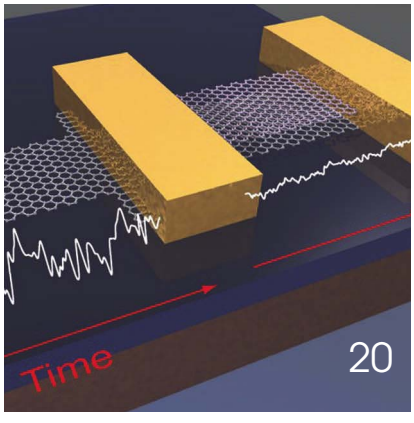
Only Actel gets you this close to zero. Any other claims of low power superiority are just that. According to their own data, Altera® and Xilinx® use between 10 and 1700 times the power of Actel IGLOO® FPGAs, depending on device and mode. Want specifics? Visit us to get the whole picture, including a video of actual measurements.

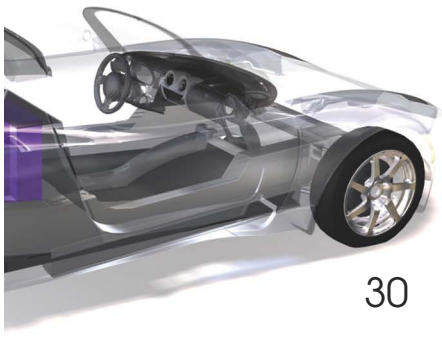
* more proof and pictures at **actel.com/power**

Actel®
POWER MATTERS

contents 5.15.08

pulse





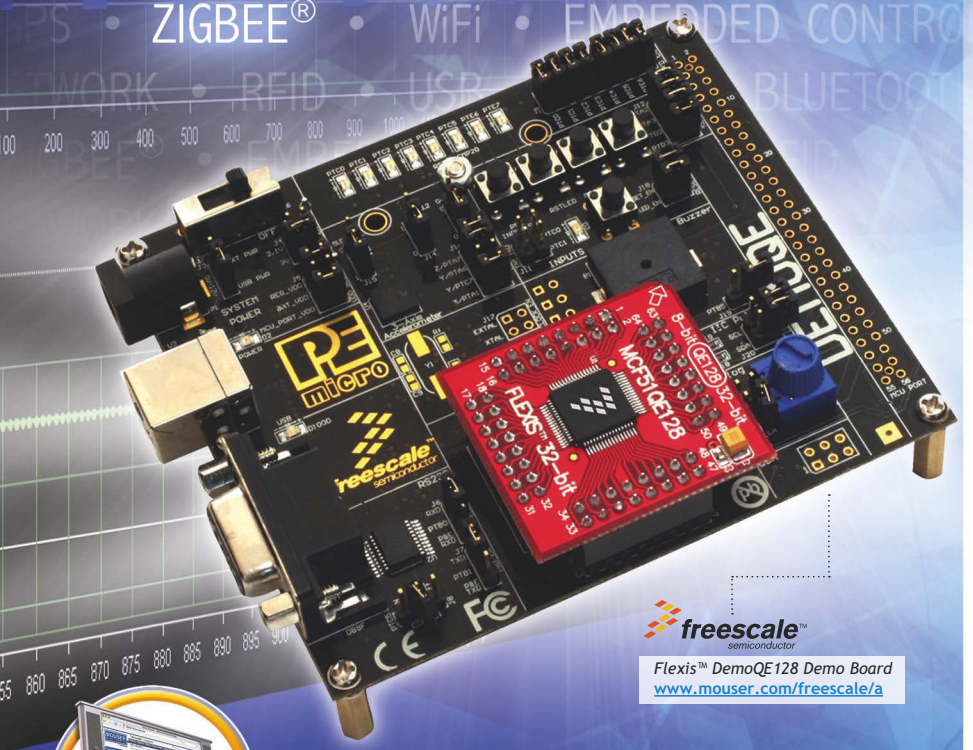
DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

EDN® (ISSN#0012-7515), (GST#123397457) is published biweekly, 26 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Mark Finkelstein, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500. *Rates for nonqualified subscriptions, including all issues: US, $165 one year; Canada, $226 one year, (includes 7% GST, GST#123397457); Mexico, $215 one year; air expedited, $398 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Agreement No. 40685520. Return undeliverable Canadian addresses to: RCS International, Box 697 STN A, Windsor Ontario N9A 6N4. E-mail: Subsmail@ReedBusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. EDN® is a registered trademark of Reed Elsevier Properties Inc, used under license. A Reed Business Information Publication/Volume 53, Number 10 (Printed in USA).*

The Newest Embedded Technologies

WiFi • USB • BLUETOOTH™ • ZIGBEE® • WLAN • NETWORK • USB • RFID • WLAN • BLUETOOTH™ • EMBEDDED CONTROL • NETWORK • RFID • USB • WLAN • GPS • BLUETOOTH™ • BLUETOOTH™ • ZIGBEE® • USB • NETWORK • RFID • USB • WLAN • BLUETOOTH™ • WiFi • ZIGBEE® • WiFi • EMBEDDED CONTROL



freescale™ semiconductor

Flexis™ DemoQE128 Demo Board
www.mouser.com/freescale/a

www.mouser.com

Over 965,000 Products Online

New Products from:

VDIP1 Module
www.mouser.com/ftdi/a

FTDI Chip

RCM4000
RabbitCore® Modules
www.mouser.com/rabbitsemi/a

RABBIT Semiconductor

MatchPort™ b/g
Embedded Device Server
www.mouser.com/lantronix/a

LANTRONIX®

The ONLY New Catalog Every 90 Days

Experience Mouser's time-to-market advantage with no minimums and same-day shipping of the newest products from more than 335 leading suppliers.

MOUSER ELECTRONICS®

a tti company

The Newest Products For Your Newest Designs

(800) 346-6873

EDN online contents

www.edn.com

ONLINE ONLY

Check out these Web-exclusive articles:

Working group plans low-power serial-DRAM interface
Proposed SPMT (serial-port-memory technology) would start by drastically simplifying handset design.
→www.edn.com/article/CA6555338

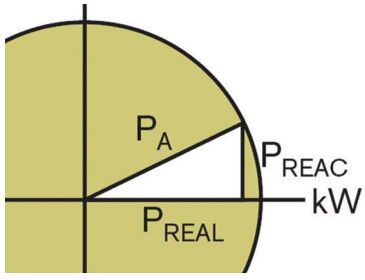
Triple core: Can AMD even the score?
Practically speaking, AMD needs to either get its clock speeds up to Intel levels or come up with a vastly more clock-efficient architecture to regain its standing as a solid competitor.
→www.edn.com/080515toc1

AMD: holes so big Intel could drive a truck through them
I'm starting to wonder whether Hector Ruiz and Bob Rivet were monks in a past life because they sure do have a vow-of-silence thing going on over at AMD.
→www.edn.com/080515toc2

Software and hardware
Processor vendors now give support and development kits serious attention.
→www.edn.com/080515toc3

ROHS: still debatable
Lead-free solder consumes more energy than tin/lead-based solder in the whole life cycle, but there is no link between the harm to health and the environment and these solders, whereas the energy-consumption link to climate change is now almost proven.
→www.edn.com/080515toc4

Is it an EDA tool or a manufacturing tool?
Blaze DFM raises the question.
→www.edn.com/080515toc5



READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

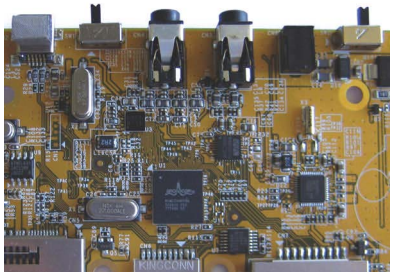
Honest energy: the danger low-power-factor loads pose for the energy grid
→www.edn.com/article/CA6544740

Boost efficiency for low-cost flyback converters
Many devices employ flyback converters because of their simplicity and low cost—not their stellar efficiency. But don't too quickly eliminate flybacks from your list of options. With a few little-known tricks, you can improve power loss by nearly 10%.
→www.edn.com/article/CA6544742

Red LEDs function as light sensors
You can build simple LED illuminators using red LEDs to sense ambient-light level.
→www.edn.com/article/CA6541376

Blu-ray's triumph provides mixed blessings
From the beginning, all HD DVD players supported features that most Blu-ray players still don't implement: built-in Ethernet ports for easy upgrades, Web-based content augmentation, and rich user-interface interactivity.
→www.edn.com/080515toc7

Current source makes novel Class A buffer
A pair of classic current sources in a totem-pole configuration enables a novel Class A buffer.
→www.edn.com/article/CA6544738



PRYING EYES

An inside look at design decisions
In Prying Eyes, we peer inside an end-user gadget, a reference design, or any other interesting electronics-enabled thing we can get a good look at. Unlike your average bill-of-materials teardown, Prying Eyes aims to illuminate the tough design decisions the engineers responsible for the design had to make. Check out this month's installment on pg 30 and then visit the complete online Prying Eyes archive.
→www.edn.com/pryingeyes

TOP 25 Electronics Distributors

Check out "The Impact of Technology Advancement on the Channel," an online-only supplement to *EDN* published in conjunction with the NEDA (National Electronic Distributors Association). Available as a 26-pg PDF, the supplement contains the Top 25 Electronics Distributors list, plus articles discussing the impact of environmental compliance and technology on the electronics supply chain.
→www.edn.com/top25distributors

Your potential. Our passion.®

Microsoft®

FAST-FORWARD YOUR MASTERPIECE.

Get your next big idea to market—faster. The built-in tools and technologies in Windows® Embedded help to accelerate development, so your teams get to put their efforts where they really count: creating the next generation of smart, connected devices. You also get Windows Embedded features that enable interoperability with industry standards and Microsoft® technologies, so you can build devices that easily connect to PCs, services, servers, and other devices. Learn more about how to fast-forward device development at: **windowsembedded.com/fastforward**

Windows® Embedded

BY PAUL RAKO, TECHNICAL EDITOR

When Web sites go bad

One of the most frustrating aspects of bad Web sites is that the contact links on the site all go to the Web team that screwed things up in the first place. Complaining to a Web team about its Web site is like complaining to the police about police brutality. My friend Dave, like all my analog-design friends, is, well, a bit different. He has an electrical-engineering degree but has spent most of his life as a software consultant. Dave is one of a few programmers I know who can program a Forth kernel for a 16-bit microcontroller. He can also, for that matter, do high-level Web programming in Perl, SQL (Structured Query Language), C, or Visual Basic. He uses a Linux machine to do his Web browsing. He uses the Opera Web browser, working on a Linux box, because it is a cross-platform product. What exasperates Dave is how poorly most Web sites run on his Linux box. Dave is also a security nut. His wife works in the IT (information-technology) department of a major semiconductor company. She even served on the InterNIC (Internet-network-information-center) committee on Web security. Dave doesn't allow his Opera Web browser to run Java or JavaScript. He also doesn't allow the Web sites he visits to drop cookies onto his machine. And he doesn't run Adobe flash under Linux. All those snazzy flash-animated sites developed with Microsoft tools for Internet Explorer don't run well on Dave's machine.

Dave complains to the Web groups about how unusable their sites are, but they don't care. Worse yet, Dave's concerns never reach the company management. The Web team makes sure that it keeps any complaints from the management, and complaints die a nice, quiet death in the Web group's trash folder. A company that does not let the public complain directly to marketing, public relations, and top management will always have a crappy product. It is no different when the product is the company's Web site. It is not hard to craft a decent Web site. You can do it even with Microsoft tools, which work only with Microsoft servers and browsers. Tim Berners-Lee, the inventor of HTML (HyperText Markup Language) and key developer of the Internet, has given his support to the W3C (World Wide Web Consortium). It runs a validator page that makes sure that any Web site does not use Microsoft-exclusive code or bad HTML or XML (Extensible Markup Language, **Reference 1**). If your company's Web site runs on that validator, and it results in no errors, it is almost certain that the Web site will work on Windows, Linux, Macintosh, and most cell phones.

A company that does not let the public complain directly to marketing, public relations, and top management will always have a crappy product.

Now, I know that *EDN* drops cookies, but it is mostly so that we can tell whether you are a unique visitor or just refreshing the page. It gives us more accurate click counts. So, I am OK with cookies, but I sure have had my fill of JavaScript and flash. The pages of NBC Sports and other media giants are so software-intensive, they bring my CAD workstation to its knees.

Web teams should look to the DigiKey Web site (www.digikey.com) to see something that just plain works. It is simple, some might even call it ugly, but it unfailingly delivers the goods. Web teams should also access their Web pages over a dial-up and a 384-kbps DSL (digital-subscriber-line) modem. When I was at National Semiconductor, the Web team operated in the corporate headquarters and had a separate network that did not use the company's servers; it was just a DSL link to the outside world. The team staged any changes on hidden servers, tried everything out over the separate network, and put the pages out "live" only when the team members were happy. There would be a lot more good Web sites in the world if the complaint went to the chief executive officer rather than the webmaster. EDN

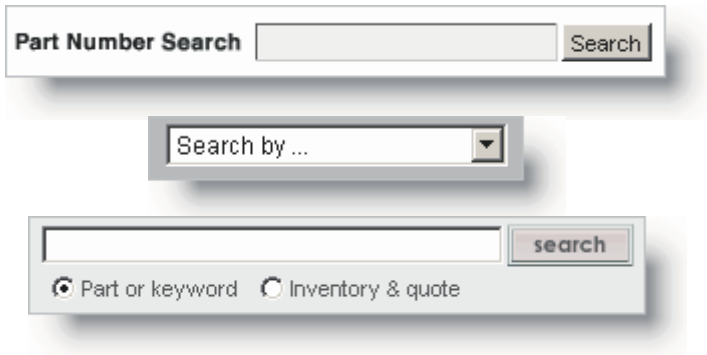
REFERENCE

1 www.w3.org/QATools.

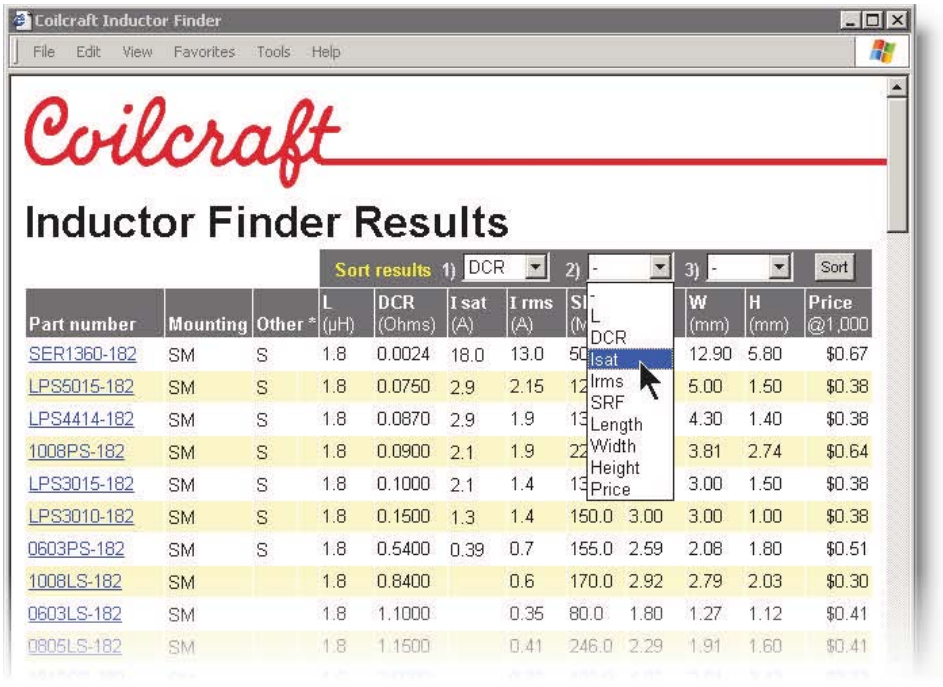
Contact me at paul.rako@edn.com.

MORE AT EDN.COM

Go to www.edn.com/080515ed and click on Feedback Loop to post a comment on this column.



Their sites have search engines. Ours has a find engine.



On most inductor web sites, their search engine results in more aggravation than answers.

But Coilcraft's web site is different.

In seconds, our Inductor Finder will show you all the parts that meet your electrical and size requirements. You can sort the results by your most important parameters. Compare pricing. Even analyze the core and winding losses of up to four different power inductors!

You'll find lots of other design tools to help you choose the perfect part. And then request free samples with just a few clicks.

So quit searching for magnetics and start finding them at **www.coilcraft.com**!

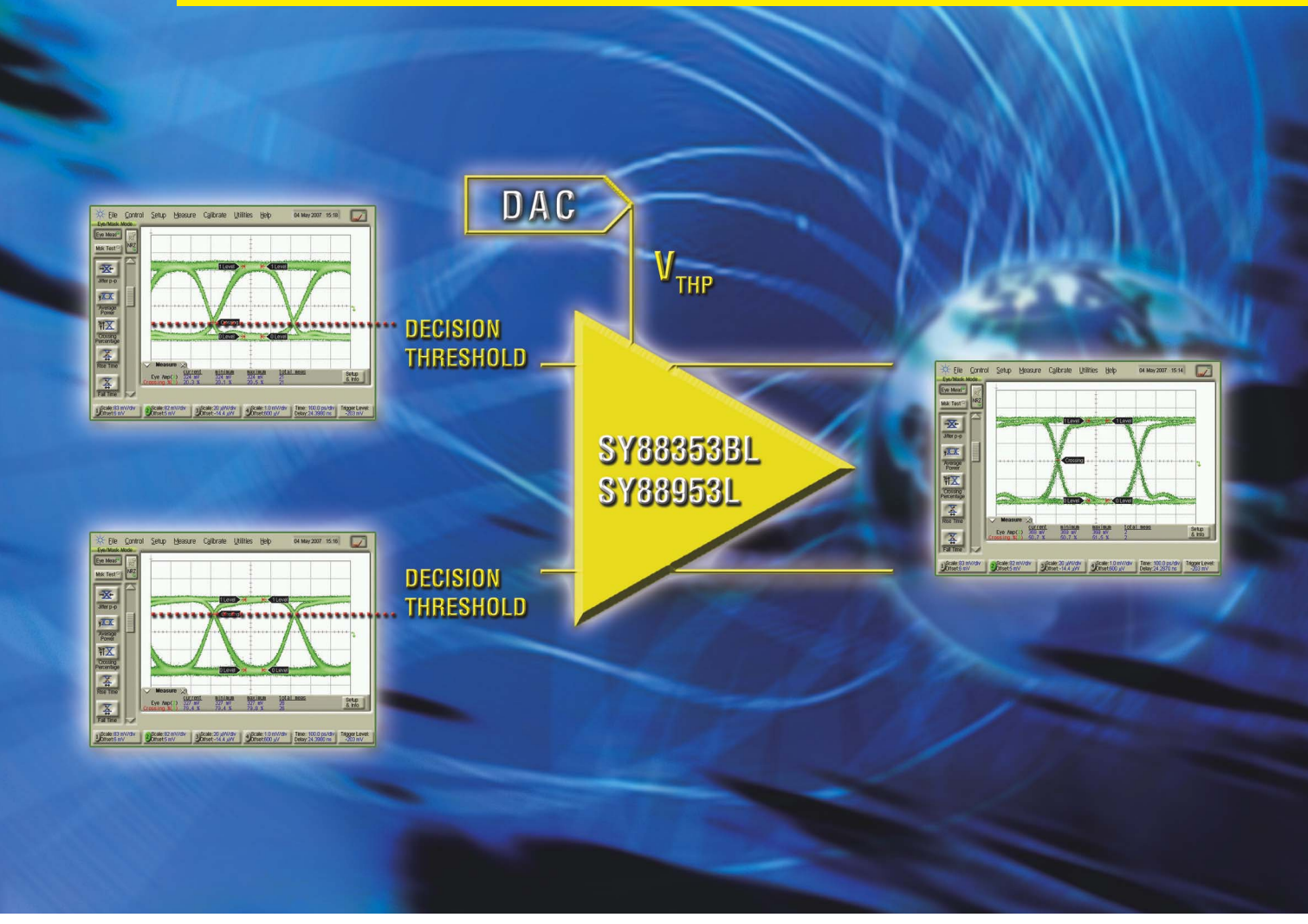
ORDER DIRECT
BUY.COILCRAFT.COM
800-322-2645
OVERNIGHT DELIVERY ORDER BY 5
RoHS COMPLIANT

Coilcraft®

www.coilcraft.com 800/322-2645

Beautify Your Eye On The Fly

3.3V, 3.2Gbps/10.7Gbps Limiting Post Amplifier with Programmable Decision Threshold



Key Benefits:

- Compensates for asymmetrical noise
- Eliminates input DC offsets in DC-coupled applications
- Decision threshold can be adjusted dynamically
- Minimizes jitter and improves BER
- Can improve sensitivity up to 3dBm
- Wide operating data range: 155Mbps - 3.2Gbps/10.7Gbps
- Tiny 3mm x 3mm MLF® package to save space and cost
- Low-noise CML output with loss-of-signal indicator

For more information, contact your local Micrel sales representative or visit us at: www.micrel.com/ad/sy88353bl.

Applications Support & Evaluation Boards:
1(408) 955-1690, hbwhelp@micrel.com

Applications:

- WDM Systems
- SONET
- Fibre Channel
- Gigabit Ethernet

MICREL®
Innovation Through Technology™

www.micrel.com

EDN

PRESIDENT, BOSTON DIVISION, REED BUSINESS INFORMATION
Mark Finkelstein, mark.finkelstein@reedbusiness.com
1-781-734-8431

PUBLISHER, *EDN* WORLDWIDE
Russell E Pratt, 1-781-734-8417;
rpratt@reedbusiness.com
ASSOCIATE PUBLISHER, *EDN* WORLDWIDE
Judy Hayes, 1-408-345-4437;
judy.hayes@reedbusiness.com
VICE PRESIDENT, EDITORIAL DIRECTOR
Karen Field, 1-781-734-8188;
kfield@reedbusiness.com
EDITOR-IN-CHIEF, *EDN* WORLDWIDE
Rick Nelson, 1-781-734-8418;
rnelson@reedbusiness.com
EXECUTIVE EDITOR
Ron Wilson, 1-408-345-4427;
ronald.wilson@reedbusiness.com
MANAGING EDITOR
Amy Norcross
1-781-734-8436; fax: 1-303-265-3017;
amy.norcross@reedbusiness.com
EDITOR-IN-CHIEF, EDN.COM
Matthew Miller
1-781-734-8446; fax: 1-303-265-3017;
mdmiller@reedbusiness.com
SENIOR ART DIRECTOR
Mike O'Leary
1-781-734-8307; fax: 1-303-265-3021;
moleary@reedbusiness.com
ANALOG
Paul Rako, Technical Editor
1-408-745-1994; paul.rako@edn.com
EMBEDDED SYSTEMS
Warren Webb, Technical Editor
1-858-513-3713; fax: 1-858-486-3646;
wwebb@edn.com
MASS STORAGE, MULTIMEDIA, PCs, AND PERIPHERALS
Brian Dipert, Senior Technical Editor
1-916-760-0159; fax: 1-303-265-3187;
bdipert@edn.com
MICROPROCESSORS, DSPs, AND TOOLS
Robert Cravotta, Technical Editor
1-661-296-5096; fax: 1-303-265-3116;
rcravotta@edn.com
NEWS
Suzanne Deffree, Managing Editor
1-631-266-3433; sdeffree@reedbusiness.com
POWER SOURCES, ONLINE INITIATIVES
Margery Conner, Technical Editor
1-805-461-8242; fax: 1-805-461-9640;
mconner@reedbusiness.com
SEMICONDUCTOR MANUFACTURING AND DESIGN
Ann Steffora Mutschler, Senior Editor
1-408-345-4436; ann.mutschler@reedbusiness.com
DESIGN IDEAS EDITOR
Charles H Small
edndesignideas@reedbusiness.com
SENIOR ASSOCIATE EDITOR
Frances T Granville, 1-781-734-8439;
fax: 1-303-265-3131;
f.granville@reedbusiness.com
ASSOCIATE EDITOR
Maura Hadro Butler, 1-617-276-6523;
mbutler@reedbusiness.com
EDITORIAL/WEB PRODUCTION
Diane Malone, Manager
1-781-734-8445; fax: 1-303-265-3024
Steve Mahoney, Production/Editorial Coordinator
1-781-734-8442; fax: 1-303-265-3198
Melissa Annand, Newsletter/Editorial Coordinator
Contact for contributed technical articles
1-781-734-8443; fax: 1-303-265-3279
Adam Odoardi, Prepress Manager
1-781-734-8325; fax: 1-303-265-3042

CONTRIBUTING TECHNICAL EDITORS
Dan Strassberg, strassbergedn@att.net
Nicholas Cravotta, editor@nicholascravotta.com
COLUMNISTS
Howard Johnson, PhD; Bonnie Baker;
Joshua Israelsohn; Pallab Chatterjee
PRODUCTION
Dorothy Buchholz, Group Production Director
1-781-734-8329
Kelly Jones, Production Manager
1-781-734-8328; fax: 1-303-265-3164
Linda Lepordo, Production Manager
1-781-734-8332; fax: 1-303-265-3015

EDN EUROPE
Graham Prophet, Editor, Reed Publishing
The Quadrant, Sutton, Surrey SM2 5AS
+44 118 935 1650; fax: +44 118 935 1670;
gprophet@reedbusiness.com

EDN ASIA
Raymond Wong, Managing Director/
Publishing Director
raymond.wong@rbi-asia.com
Kirtimaya Varma, Editor in Chief
kirti.varma@rbi-asia.com

EDN CHINA
William Zhang, Publisher and Editorial Director
wmzhang@idg-rbi.com.cn
John Mu, Executive Editor
johnmu@idg-rbi.com.cn

EDN JAPAN
Katsuya Watanabe, Publisher
k.watanabe@reedbusiness.jp
Ken Amemoto, Editor-in-Chief
amemoto@reedbusiness.jp

The EDN *Editorial Advisory Board serves as an industry touchstone for the editors of* EDN *worldwide, helping to identify key trends and voicing the concerns of the engineering community.*

EDN, 225 Wyman St, Waltham, MA 02451. **www.edn.com**. Phone 1-781-734-8000. **Address changes or subscription inquiries:** phone 1-800-446-6551; fax 1-303-470-4280; subsmail@reedbusiness.com. For a free subscription, go to **www.getfreemag.com/edn**. Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Include your mailing label.

Reed Electronics Group

ACM/EDAC/IEEE 45th DESIGN AUTOMATION CONFERENCE
JUNE 8-13, 2008 • ANAHEIM, CA • WWW.DAC.COM

Where electronic design meets...

Mark your calendars for the 45th Design Automation Conference (DAC) at the Anaheim Convention Center, June 8-13, 2008, in Anaheim, California, USA.

Only DAC Offers:

- A robust technical program covering the latest research developments and trends for the design of SoCs, FPGAs, ASICs, digital ICs and more.
- Worldwide attendance from leading electronics companies and universities.
- Over 250 companies displaying electronic design technologies and services.

Highlights Include:

- Wireless Theme sessions
- Management Day on Tuesday, June 10
- Paper sessions featuring leading technical research
- New "iDesign" and WACI sessions
- Dynamic Panels Sessions
- DAC Pavilion Panels on the show floor
- 19 collocated events and workshops
- Full-day and Hands-on Tutorials
- *New! Exhibitor Forum on the show floor*

2008 Keynotes:

- **Justin R. Rattner**, Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp.
  EDA for Digital, Programmable, Multi-Radios
  Tuesday, June 10
- **Sanjay K. Jha,** COO and president of Qualcomm CDMA Technologies
  Challenges on Design Complexities for Advanced Wireless Silicon Systems
  Wednesday, June 11
- **Jack Little,** President, CEO, and a Co-founder of The MathWorks, Inc.
  Idea to Implementation: A Different Perspective on System Design
  Thursday, June 12

Register on or before May 19th to receive 20% off Conference Registration or for a FREE Exhibit-Pass!

REGISTER ON-LINE TODAY: www.dac.com

Sponsored by: acm EDA CONSORTIUM IEEE

Supported by: CEDA IEEE CIRCUITS & SYSTEMS SOCIETY CANDE sigda SSCS

In Technical Cooperation with:

45 YEARS

DESIGN AUTOMATION CONFERENCE

PERIPHERAL SUPPORT ICs

OUR SEMICONDUCTOR SOLUTIONS RESOURCE Volume 8, Issue 3

Contents

High Performance *i*CMOS® Switches and Multiplexers Enable Critical System Functions Everywhere

Analog Devices offers a broad portfolio of robust ±15 V switches and multiplexers that are used in a wide range of applications where system reliability is critical, including industrial and instrumentation, medical, consumer, communications, and automotive systems. Leveraging the patented *i*CMOS manufacturing process technology, ADI's array of switches and multiplexers offers industry-leading performance in very small form factors to enable board area space savings.

Automatic Test Equipment Applications

For ATE applications with single-ended or differential inputs, ADI offers a choice of multiplexers with single four, eight, and 16 channels or differential four and eight channels. The ADG1406 is a ±15 V, 16:1 multiplexer, and the ADG1407 is a differential 8:1 multiplexer. Both offer low on resistance of 8 Ω with <1 Ω on-resistance flatness over the full signal range and are available in space-saving 5 mm × 5 mm LFCSP packages.

Medical Applications

In medical applications such as line-powered ECGs, where the requirements are generally for low R_{ON}, dual-supply operation switches, the ADG1411 (4 × SPST) offers superior on resistance of 1.5 Ω and R_{ON} flatness of 0.28 Ω over the full signal range. This level of performance assists in minimizing signal loss and distortion of the signal through the switch—especially important when switching gains for op amps. The ADG1411 is available in 4 mm × 4 mm LFCSP packaging, suitable for both portable and benchtop systems.

Industrial Applications

Industrial design engineers require analog switches that support faster sampling, increased performance, lower power dissipation, and a smaller footprint. The ADG1201 SPST and ADG1219 SPDT switches meet these requirements by offering ultralow capacitance, charge injection, and leakage at ±15 V operation. Both have <1 pC charge injection and low leakage of <1 nA at 125°C and are available in tiny 6-lead SOT-23 packages.

For more information, go to *www.analog.com/icmos*.

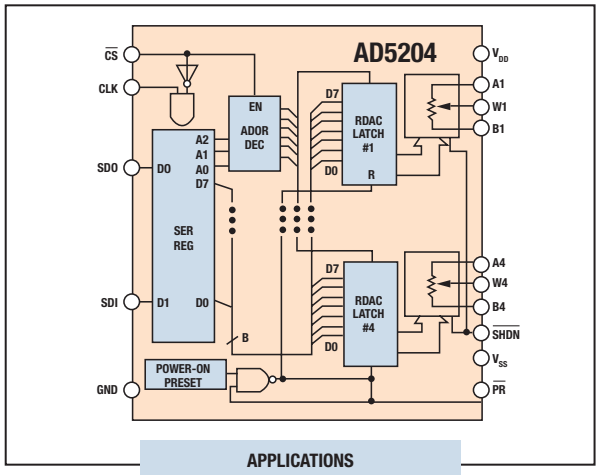
Part Number	Function	R_{ON} Typ (Ω)	Q_{INJ} Typ (pC)	On Leakage Typ (nA)	Package (mm)	Price ($U.S.)
ADG1201, ADG1202	1 × SPST, NC, NO	120	0.3	0.02	6-lead SOT-23	1.01
ADG1411, ADG1412, ADG1413	4 × SPST, NO, NC, NO/NC	1.5	20	0.2	TSSOP, 4 × 4 LFCSP	2.66
ADG1406, ADG1407	16:1, diff 8:1 mux	8	50	0.04	TSSOP, 5 × 5 LFCSP	4.81

Order this valuable design resource to help optimize your PC board designs.

Quad Channel, 256-Position Digital Potentiometers in 5 mm × 5 mm QFN Packaging Significantly Reduce Board Space

A digital potentiometer adjusts and trims electronic circuits in the same way that variable resistors, rheostats, and mechanical potentiometers do. These compact devices can be used to calibrate system tolerances or dynamically control system parameters in cases where a fine-tuned analog output is controlled by a digital input.

The AD5204 provides 4-channel, 256-position, digitally controlled variable resistor (VR) devices. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Each channel of the AD5204 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance between the A terminal and the wiper or the B terminal and the wiper. The fixed A-to-B terminal resistance of 10 kΩ, 50 kΩ, or 100 kΩ has a nominal temperature coefficient of 700 ppm/°C. Each VR has its own VR latch, which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial input digital interface. Eleven data bits make up the data word clocked into the serial input register. The first three bits are decoded to determine which VR latch will be loaded with the last eight bits of the data word when the CS strobe is returned to logic high. A serial data output pin at the opposite end of the serial register (AD5204 only) allows simple daisy-chaining in multiple VR applications without additional external decoding logic. The AD5206 is a 6-channel solution.



APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation gain, offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, time constants
- Line impedance matching

Packaging options help you to address your system requirement trade-offs including device cost and board area. Options for both the AD5204 and AD5206 include 24-lead SOIC, TSSOP, and PDIP packages. The AD5204 is also available in 5 mm × 5 mm LFCSP for the most popular 10 kΩ resistor value.

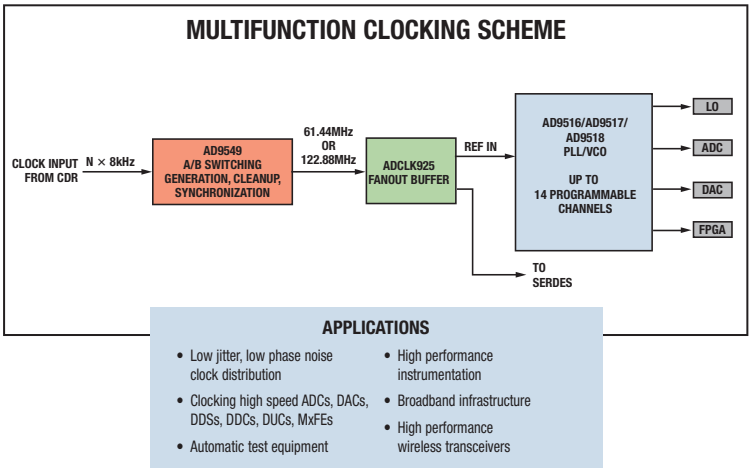
Part Number	Number of Channels	Number of Positions	Memory Type	Interface	Resistor Values (kΩ)	Voltage Range (V)	Temperature Range (°C)	Absolute Tempco (ppm/°C)	Price ($U.S.)
AD5203	4	64	Volatile	SPI	10, 100	5.5	–40 to +85	700	1.45
AD5204	4	256	Volatile	SPI	10, 50, 100	±3, 5.5	–40 to +85	700	1.50
AD8403	4	256	Volatile	SPI	1, 10, 50, 100	5.5	–40 to +125	500	2.76
AD5263	4	256	Volatile	I²C,® SPI	20, 50, 200	±5, 15	–40 to +125	30	2.55
AD5206	6	256	Volatile	SPI	10, 50, 100	±3, 5.5	–40 to +85	700	1.92
AD5233	4	64	Non-volatile	SPI	1, 10, 50, 100	±3, 5.5	–40 to +85	600	2.47
AD5253	4	64	Non-volatile	I²C	1, 10, 50, 100	±3, 5.5	–40 to +85	300	2.46
AD5254	4	256	Non-volatile	I²C	1, 10, 50, 100	±3, 5.5	–40 to +85	300	2.55

Flexible Clocking Scheme Accommodates Multiple Wireless Standards

To establish a clean and stable clock in wireless systems, designers typically employ a standard set of multiple discrete components including FPGA, filters, VCXO, PLL, and various clock distribution circuitry. However, this approach is undesirable because it often yields a complicated, high cost, low reliability clocking scheme, and consumes a large portion of the PCB area. In contrast, integrating critical timing functions onto higher function clock devices translates to using fewer components for lower overall cost, increased reliability, and a smaller footprint. As shown in the diagram below, multiple clock ICs may be combined to form a complete multifunction timing solution that addresses clock cleanup, generation, synchronization, and distribution, to meet the most stringent system requirements.

In a remote radio unit (RRU), the incoming signal is cleaned up and then delivered to a clock generator to translate the frequency outputs to other system components. The ultraclean signal from the buffer goes through a SERDES to be sent back upstream. This clocking platform is ideal for digitizing a signal across multiple wireless standards, such as WiMAX, W-CDMA, CDMA2000, and CDMA.

The AD9549 clock generator/synchronizer cleans up a CDR clock using a digital PLL with a programmable loop bandwidth down to 0.1 Hz. The device provides reference monitoring and holdover functions. It delivers integrated jitter of <1 ps rms.



An ultrafast 1:2 clock buffer, the ADCLK925, boasts fast output rise and fall times of 60 ps to maximize bandwidth and signal integrity. In addition, only 60 fs of random jitter is added on the outputs. The buffer distributes clean copies of the signal to both a SERDES and a flexible multioutput clock generator.

The AD9516, AD9517, and AD9518, all with on-chip VCXO, offer excellent close-in phase noise performance when clocking multiple system components. The flexibility in selecting from multiple logic types and frequency combinations creates an ideal solution that can be used in various wireless systems. Five versions of each product are available with VCOs tuned from 1.45 GHz to 2.95 GHz.

Clock Generation ICs

Part Number	Outputs	Dividers	Delay Lines	Package	Price ($U.S.)
AD9516-x	6 LVPECL, 4/8 LVDS/CMOS	5	4	9 mm × 9 mm, 64-lead LFCSP	12.50
AD9517-x	4 LVPECL, 4/8 LVDS/CMOS	4	4	7 mm × 7 mm, 48-lead LFCSP	11.40
AD9518-x	6 LVPECL	3	None	7 mm × 7 mm, 48-lead LFCSP	9.85

Clock Buffers

Part Number	Number of Inputs	Number of Outputs	Max Clock Input (GHz)	Output Logic	Random Jitter (ps rms)	Price ($U.S.)
ADCLK905	1	1	6	ECL, PECL, LVPECL	0.06	5.60
ADCLK907	2	2	6	ECL, PECL, LVPECL	0.06	6.75
ADCLK914	1	1	6	HVDS	0.1	6.95
ADCLK925	1	2	6	ECL, PECL, LVPECL	0.06	5.95

Design the jitter out of your circuit with the help of ADI's ADIsimCLK™ free online design tool. To begin, visit *www.analog.com/ADIsimCLK*.

"Network Clock: How to Achieve Maximum System Up Time" at *www.analog.com/onlineseminars*.

Optimizing Signal Chain Performance with Voltage References

As a point of reference for converter accuracy, voltage references play a critical role in overall system performance. Providing the comparison for all other measurements, a voltage reference's accuracy, noise, and stability (among other specifications) are vital to allowing the converter to produce an accurate measurement (for ADC) or output (for DAC). Using a discrete voltage reference is often desirable when best-in-class tempco, hysteresis, and long-term drift performance are important to the application. Analog Devices offers a wide range of voltage references, from <3 ppm/°C for test, measurement, and instrumentation applications to >50 ppm/°C for power delivery and power management applications.

Part Number	V_0 (V)	Initial Accuracy (%)	Tempco (ppm/°C)	Output Noise (μV p-p)	Supply Voltage (V)	Package	Price ($U.S.)
ADR121, ADR125, ADR127	2.5, 5, 1.25	0.12, 0.24	9, 25	10, 20, 5	2.7 to 18	6-lead TSOT	0.77, 1.19
ADR130	0.5, 1	0.35, 0.7	25, 50	3, 6	2 to 18	6-lead TSOT	0.97, 1.25
ADR42x, ADR43x, ADR44x	2.048, 2.5, 3, 4.096, 4.5, 5	0.05, 0.15	3, 10	1 to 7.5	4.5 to 18	8-lead MSOP, 8-lead SOIC	2.65, 3.05
AD586	5	0.04, 0.05, 0.1, 0.2	2, 5, 10	4	10 to 36	8-lead PDIP, 8-lead SOIC	2.86, 6.91
REF19x	2.048, 2.5, 3, 3.3, 4.096, 4.5, 5	0.04, 0.33	2, 5, 10, 20, 25	20 to 50	3 to 15	8-lead PDIP, 8-lead SOIC, 8-lead TSSOP	1.36, 2.59

"Driving Precision Converters: How to Select the Best Voltage Reference and Amplifier for Your ADC Application" at *www.analog.com/onlineseminars*.

Protect and Optimize Communications Networks with ADI's New Family of 0.8% Accuracy, Quad Channel Voltage Monitors and Sequencers

Analog Devices introduces several new quad voltage monitors and sequencers with industry-leading, highest accuracy threshold accuracy (0.8%). The 0.8% threshold accuracy specification allows low voltage rails (~1 V) to be accurately monitored and sequenced. The ADM1186 allows power-up and power-down (reverse order) sequencing in hardware using resistors and capacitors. No software support is required. Correct power supply sequencing ensures that the power supply rails come up and are powered down in the correct order and that each rail is within tolerance ensuring more reliable system performance. The cascadability of these devices provides power up and down (reverse sequence) of more than four voltage rails by cascading multiple devices. External capacitors define the time delay between the voltage rails turning on during the power-up sequence and turning the power supplies off during the power-down sequence.

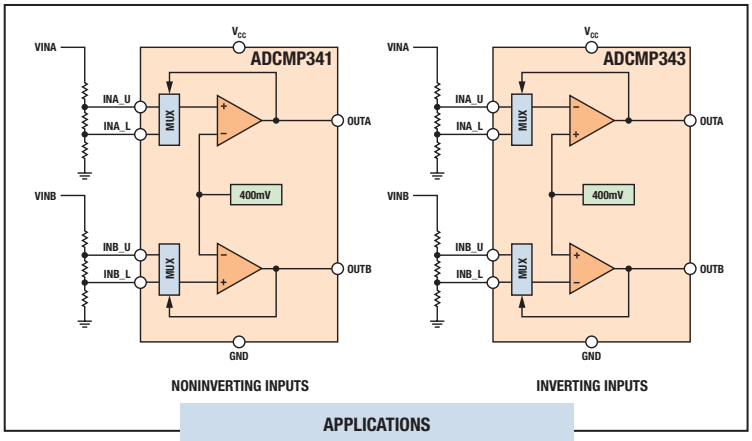
Part Number	Number of Supplies Monitored	Voltage Monitoring Accuracy	Number of Output Drivers	Sequencing		Enable Output	Sequence Delay	Package	Price ($U.S.)
				Up	Down				
ADM1184	4: cascadable	<0.8%	4	Yes	No	Open-drain	—	10-lead MSOP	2.39
ADM1185	4: cascadable	<0.8%	4	Yes	No	Open-drain	190 ms	10-lead MSOP	1.20
ADM1186-1	4: cascadable	<0.8%	4	Yes	Yes	Open-drain	Cap adj	20-lead QSOP	3.80
ADM1186-2	4	<0.8%	4	Yes	Yes	Open-drain	Cap adj	16-lead QSOP	2.98

ADI Continues to Grow Its Low Power Comparator Portfolio with Dual Comparators that Feature Integrated Reference and Programmable Hysteresis

Lower power comparators are ideal for power sensitive applications such as battery-powered equipment. The ADCMP341 and ADCMP343 ICs combine two low power, low voltage comparators with a 400 mV reference in a tiny 5-lead SOT-23 package. Operating within a supply range of 1.7 V to 5.5 V, the devices only draw 6.5 μA typical—making them ideal for low voltage system monitoring and portable applications. Hysteresis is determined using three resistors in a string configuration with the upper and lower tap points connected to the INA_U and INA_L pins of each comparator, respectively. The comparator's output internally selects which pin is connected to the comparator inputs. A change of state in the comparator output will result in one of the inputs being switched into the comparator, while the other is switched out. This functionality provides the user with an easy method of setting the hysteresis. The comparator outputs are open-drain with the output stage sinking capability guaranteed greater than 5 mA over temperature. In addition, this IC family offers various features depending upon the design need—for example, the ADCMP341 has noninverting inputs while the ADCMP343 has inverting inputs. The devices are available in commercial, industrial, and automotive temperature ranges. For a complete listing of ADI comparators, visit *www.analog.com/comparators*.

Low Power Comparator Family Features

- Low quiescent current: 6.5 μA typical
- Supply range: 1.7 V to 5.5 V
- 400 mV reference: ±0.275% threshold accuracy
- Input range includes ground
- User programmable hysteresis via resistor string
- Low input bias current: ±5 nA maximum
- Open-drain outputs
- Supports wire-AND'ed connections
- Input polarities (noninverting and inverting)
- Package: small, 8-lead SOT-23



APPLICATIONS

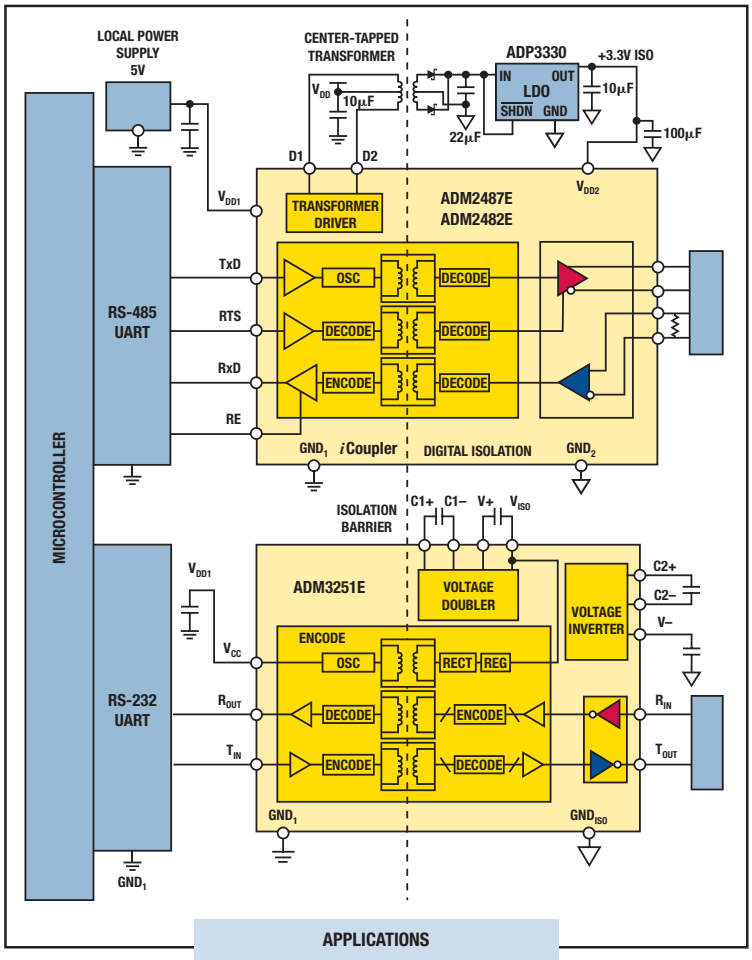
- Portable applications
- Li-Ion monitoring
- Handheld instruments
- LED/relay driving
- Optoisolator driving
- Control systems

Part Number	Number per Package	Reference Accuracy (±%)	Supply Voltage (V)	Logic I/O	Input Range (V)	Propagation Delay Typ (μs)	Hysteresis	Package	Price ($U.S.)
ADCMP341	2	0.275	1.7 to 5.5	Open-drain	0 to V_{CC}	10.0	Adjustable	8-lead SOT-23	0.90
ADCMP343	2	0.275	1.7 to 5.5	Open-drain	0 to V_{CC}	10.0	Adjustable	8-lead SOT-23	0.90
ADCMP350	1	3.5	2.25 to 5.5	Open-drain, active low	0 to 22	5.0	Internal	4-lead SC70	0.31
ADCMP354	1	3.5	2.25 to 5.5	Open-drain, active high	0 to 22	5.0	Internal	4-lead SC70	0.31
ADCMP356	1	3.5	2.25 to 5.5	Push-pull, active high	0 to 22	5.0	Internal	4-lead SC70	0.31
ADCMP361	1	0.275	1.7 to 5.5	Open-drain	0 to V_{CC}	10.0	Internal	5-lead SOT-23	0.60
ADCMP370	1	—	2.25 to 5.5	Open-drain	0 to 22	5.0	Internal	5-lead SOT-23	0.28
ADCMP371	1	—	2.25 to 5.5	Push-pull	0 to 22	5.0	Internal	5-lead SOT-23	0.28
ADCMP670	2	1.50	1.7 to 5.5	Open-drain	0 to 6	10.0	Internal	6-lead SOT-23	1.40
CMP04	4	—	5	Open-collector	V_{CC} to 1.5	1.3	—	14-lead SOIC	4.75

Protect Your Valuable Communications Networks with ADI's Family of RS-232 and RS-485 Digitally Isolated ICs

The RS-485 and RS-232 bus standards are the most widely used physical layer bus designs in industrial and instrumentation and medical applications. To improve system reliability within a noisy environment and protect against voltage spikes and ground loops, isolation is required between the RS-485/RS-232 cable network and the systems connected to it. Power isolation is obtained through the use of an isolated dc-to-dc power supply or Analog Devices *iso*Power® integrated dc-to-dc converters. Signal isolation is implemented using Analog Devices' *i*Coupler® technology. ADI provides integrated isolated RS-485 and RS-232 transceivers to solve these problems.

In addition, visit *www.analog.com/rs485* and *www.analog.com/rs232* for more information.



APPLICATIONS

- Industrial fieldbus networks
- Factory automation systems
- Motor control
- Building controls
- Medical

"Digital Isolation Tips and Techniques" at *www.analog.com/onlineseminars.*

Part Number	Protocol	FD/HD	Data Rate	Isolation Rating (V rms)	Temperature Range (°C)	Integrated *iso*Power	Integrated Transformer Driver	Package	Price ($U.S.)
ADM2483	RS-485	HD	500 kbps	2500	–40 to +85	No	No	16-lead wide SO	3.00
ADM2485	RS-485	HD	16 Mbps	2500	–40 to +85	No	Yes	16-lead wide SO	5.50
ADM2486	RS-485	HD	20 Mbps	2500	–40 to +85	No	No	16-lead wide SO	4.98
ADM2490E	RS-485	FD	16 Mbps	5000	–40 to +105	No	No	16-lead wide SO	4.50
ADM2491E	RS-485	FD/HD	16 Mbps	5000	–40 to +85	No	No	16-lead wide SO	4.70
ADM2487E	RS-485	FD/HD	500 kbps	2500	–40 to +85	No	Yes	16-lead wide SO	3.60
ADM2482E	RS-485	FD/HD	15 Mbps	2500	–40 to +85	No	Yes	16-lead wide SO	4.60
ADM3251E	RS-232	—	460 kbps	2500	–40 to +85	Yes	No	20-lead wide SO	2.99

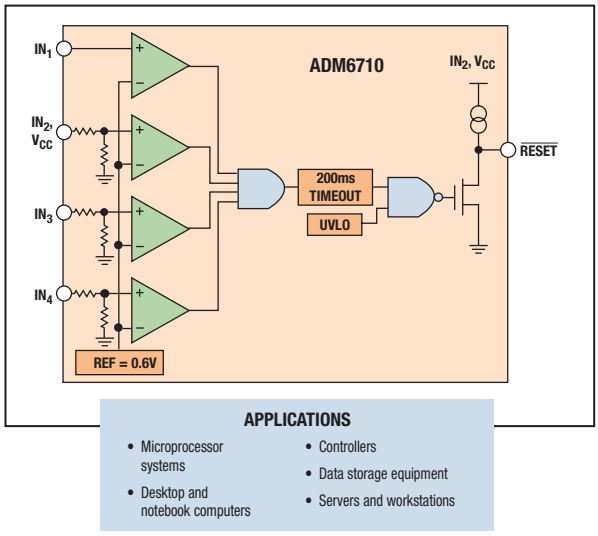
ADI's High Accuracy Multivoltage Supervisor ICs Monitor Low Voltage Core Supplies for Peak Performance

Accurately monitoring the supply voltage of a microprocessor is critical to achieving the levels of performance and output required by today's sophisticated electrical equipment. To meet these needs, ADI's family of voltage monitors includes dual, triple, and quad variants that accommodate a wide range of voltage inputs.

The ADM6710 is a low voltage, high accuracy, microprocessor supervisory circuit capable of monitoring up to four system supply voltages. Should an input drop below its associated threshold, an active low output asserts. The output is open-drain with a weak internal pull-up to the monitored IN2 or V_{CC} supply, typically 10 μA. Subsequent to all voltages rising above the selected threshold, the reset remains low for the reset timeout period (140 ms minimum).

ADM6710 Features

- Accurate monitoring of up to four power supply voltages
- Five factory set threshold options: 1.8 V, 2.5 V, 3.0 V, 3.3 V, 5 V
- Adjustable input monitors down to 0.62 V (1.5% accuracy)
- Reset timeout: 140 ms (minimum)
- Open-drain reset output: 10 μA internal pull-up
- Reset output stage: active low, valid to IN1 = 1 V or IN2 = 1 V
- Low power consumption: 35 μA
- Power supply glitch immunity
- Specified from –40°C to +85°C
- Package: 6-lead SOT-23

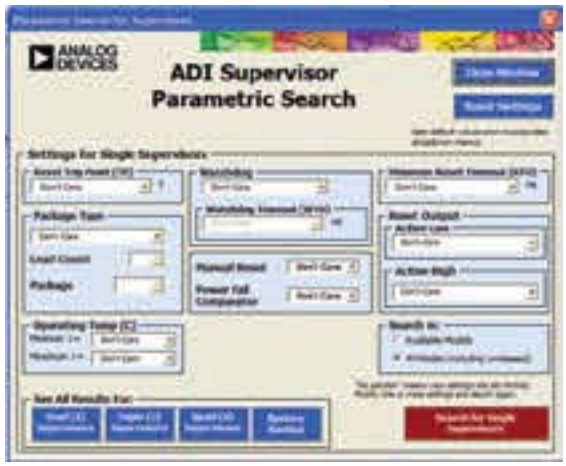


For more information on ADI's complete portfolio of supervisory products, visit *www.analog.com/supervisory*.

Part Number	Number of Monitored Voltages	Reset Threshold (V)	Min Reset Timeout (ms)	Reset Output Stage	Manual Reset Capability	Typical Watchdog Timeout (sec)	Package	Price ($U.S.)
ADM13305	2	0.6 (adjustable), 1.68, 2.25, 2.93, 4.55	140	Active high, push-pull, active low, push-pull	Yes	1.6	8-lead NSOIC	0.95
ADM13307	3	0.6 (adjustable), 1.25 (adjustable), 1.68, 2.25, 2.93, 4.55	140	Active high, push-pull, active low, push-pull	Yes	—	8-lead NSOIC	0.98
ADM6710	3 or 4	0.62 (adjustable), 1.58, 1.67, 2.19, 2.32, 2.63, 2.78, 2.93, 3.08, 4.38, 4.63	140	Active low, open-drain	No	—	6-lead SOT-23	1.60
ADM1184	4	0.6 (adjustable)	100	Active high, open-drain	No	—	10-lead MSOP	2.39

New Online Supervisory Selection Tools Take the Guess Work Out of Selecting the Perfect Supervisory IC for Your Design

ADI's new supervisory IC selection tools enable the design engineer to perform customized parametric searches of ADI's extensive supervisory product database. Searchable parameters include trip points, reset timeouts, watchdog timeouts, reset types, and an array of other critical features. In addition, this free downloadable tool provides a convenient cross-reference matrix between our competitors' parts and ADI's. To start using the new supervisory IC selection tool today, visit *www.analog.com/supervisory-tool*.



For a complete list of ADI's online tools and other helpful design resources, go to *www.analog.com/designcenter*. Popular tools include:

ADIsimADC™
www.analog.com/ADIsimADC
Simulate system behavior using many critical specifications of high speed data converters, including offset, gain, sample rate, bandwidth, jitter, latency, and both ac and dc linearity.

NI Multisim™ Analog Devices Edition
www.analog.com/multisim
Jointly developed between NI and ADI, this tool provides an intuitive environment for capturing and simulating analog circuits.

ADIsimOpAmp™
www.analog.com/ADIsimOpAmp
This tool will help with the selection, evaluation, and troubleshooting of voltage feedback op amps.

ADIsimPLL™ and ADIsimDDS™
www.analog.com/ADIsimPLL and
www.analog.com/ADIsimDDS
These two circuit design tools allow the designer to simulate and evaluate complete RF circuits using either PLL or DDS frequency synthesis products.

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

Printed in the U.S.A. SB07448-90-4/08

www.analog.com

ANALOG DEVICES

EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Stackable receiver enables position tracking

As transportable embedded systems become commonplace, designers are looking for economical ways to integrate global-positioning equipment to track movements and deter theft. To target these applications, Micro/sys recently released the USB1700, a GPS (global-positioning-system)-receiver board in a form factor one-quarter the size of the PC/104 footprint. The ROHS (restriction-of-hazardous-substances) module provides designers with 12-channel, WAAS (wide-area-augmentation-system)-capable GPS functions for space-sensitive applications. The integrated GPS technology offers fast start-up and high performance in foliage-canopy, multipath, and urban-canyon environments. The board comes with a passive antenna.

The new USB1700 GPS-receiver board comes in a form factor one-quarter the size of the standard PC/104 footprint.

The USB1700 physically conforms to a new form factor, which StackableUSB (www.stackableusb.org) defines. StackableUSB is a fairly recent standard that uses USB communications between a single-board computer and peripheral-I/O cards in a stack similar to PC/104. Depending on the design, the CPU card can support 10 peripheral I/O cards—five on the top and five on the bottom—without the use of a hub board. At 1.85×1.78 in., the USB1700 is one-fourth the size of a standard card, resulting in improved cooling and smaller packaging. To accommodate the smaller StackableUSB form factors, the company added a fifth stabilizing hole to the 104-footprint definition. Prices for the basic USB1700 start at $230 (one).

—by Warren Webb

▷**Micro/sys Inc**, www.embeddedsys.com.

FEEDBACK LOOP

"EDA has always been 'broken,' and, as long as the technology continues to evolve, the EDA tool designed last year is going to be difficult to wield effectively on this year's problem."

—Web-site visitor Dave J at www.edn.com/080515p1. Add your comments.

AMD releases dual- and triple-core desktop processors

To bring multicore technology to desktop processors that handle multithreaded-digital-entertainment workloads, microprocessor challenger AMD (Advanced Micro Devices) recently introduced three Phenom X3 triple-core processors. With the company's 780 series chip set, the new devices allow a full HD (high-definition) experience and good gaming and digital performance.

With these processors, AMD aims to free users from the need to weigh trade-offs between graphics and processors when purchasing a PC, given that the proliferation of digital-media devices and entertainment changes the way consumers use PCs and creates stronger demand on processing and graphics capabilities.

AMD based the multicore technology on the Direct Connect architecture, which has allowed the company to bring these triple-core desktop processors to market with benefits similar to those available with AMD's Phenom X4 quad-core processors. The triple-core processors have better performance for multitasking and multithreaded digital-media and game applications than do dual-core processors at the same clock speed, according to the company. The 2.4-GHz Phenom X3 8750, 2.3-GHz 8650, and 2.1-GHz 8450 triple-core processors sell for $195, $165, and $145, respectively.

—by Ann Steffora Mutschler

▷**Advanced Micro Devices**, www.amd.com.

Multiprocessor system sports as many as four coherent, multithreaded cores

MIPS Technologies' multithreaded, multiprocessor, coherent-processing MIPS32 1004K licensable-IP (intellectual-property) platform supports as many as four single- or double-threaded processor cores that connect through a coherence manager. The nine-stage-pipeline architecture supports a worst-case 800-MHz base-core operating frequency in a 65-nm TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) general-purpose process. The architecture implements a dual-core, dual-threaded configuration for a total of four threads.

The architecture also has 32-kbyte caches for each core, a coherence manager, and a global-interrupt controller. The devices are available with 1004Kc integer and 1004Kf floating-point versions of the core, and they both support Revision 1 of the MIPS32 DSP ASE (application-specific extension). The design-time configurability of the platform allows designers to size the instruction and data caches, TLBs (translation-look-aside buffers), scratchpad RAM, and user-defined instructions. The configuration must be the same for each core in a given implementation, however, so that the architecture can support SMP (symmetric-multiprocessing) operation with SMP-based operating systems, such as Open Source SMP Linux.

> The design-time configurability of the platform allows designers to size the instruction and data caches, TLBs, scratchpad RAM, and user-defined instructions.

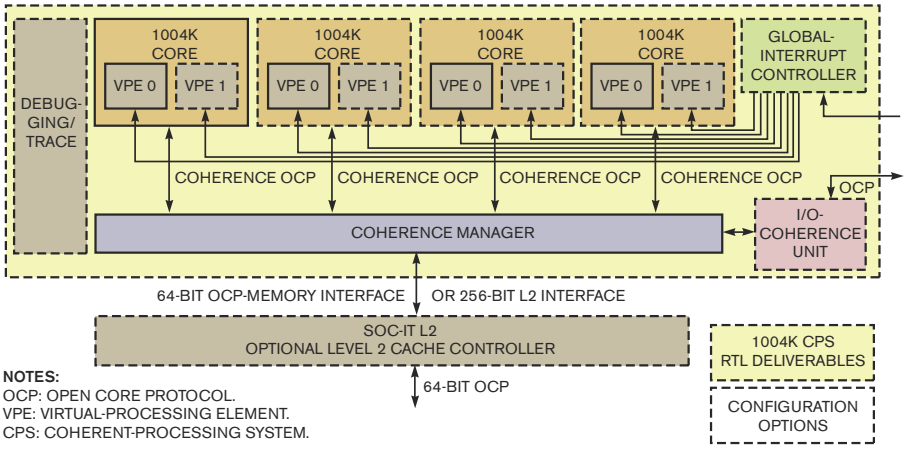
The multicore-coherence manager can manage one to four single- or dual-threaded cores, and it operates at the same clock rate as the cores, which also operate at the same clock rate. The coherence manager supports cache-to-cache transfers, speculative reads to external memory, and global-cache operations. It manages coherency using the MESI (modified/exclusive/shared/invalid) protocol, and it employs redundant tags to enable L1 cache transfers and minimize the impact on processing performance. Designers configure and control the coherence scheme through global-configuration registers.

The platform supports an optional 256-bit interface that can manage fractional-clock-rate access to an L2 memory controller. The optional I/O-coherence unit bridges noncoherent I/O-peripheral-data transfers so that the transactions are coherent within the system; it also supports per-transaction attributes for snooping L1 caches, L1 and L2 caches, noncoherent transactions, and I/O prioritization. The global-interrupt controller can route as many as 256 system-level and interprocessor interrupts to cores or VPEs (virtual-processing elements).

The SDE (software-development environment) for this platform includes the Gnu-based MIPS SDE tool chain, the MIPSsim bus-functional modeling and instruction-set simulator, and the enhanced-JTAG and PDtrace system-navigator probe with coherence awareness. The two initial versions of this core, the integer 1004Kc and the floating-point 1004Kf, will be available for licensing this quarter.

—by Robert Cravotta

▷**MIPS Technologies**, www.mips.com.



The MIPS32 1004K architecture implements a dual-core, dual-threaded configuration for a total of four threads.

DILBERT By Scott Adams

Flexible Clock Generators

Multiple I/O-V and Programmability Ease System Design

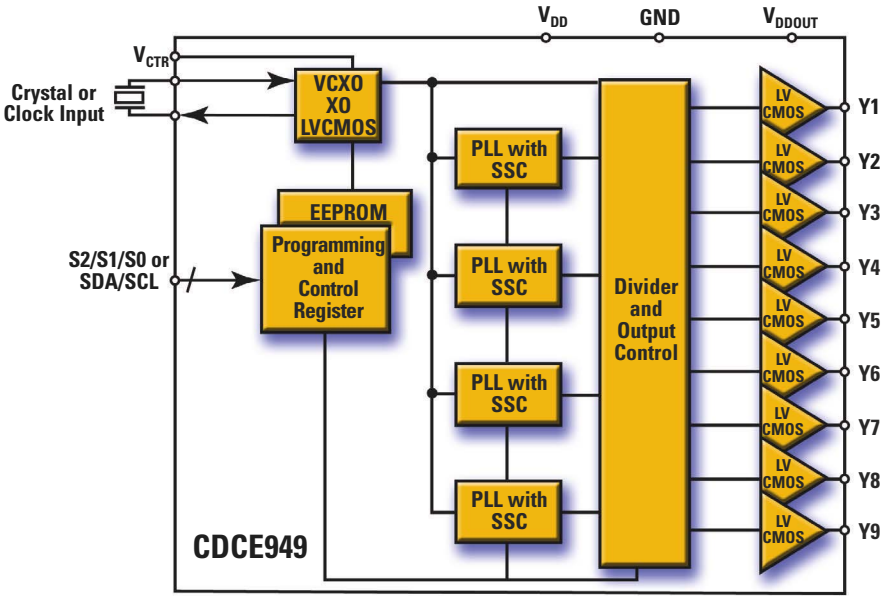
High-Performance Analog>>Your Way™

Applications

- Digital media systems (audio/video)
- GPS receivers
- TI DSP, OMAP™ and DaVinci™ media processors

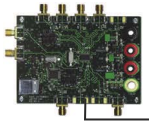
Features

- Spread Spectrum Clocking (SSC) reduces affects of EMI
- I^2C and EEPROM programmability
- On-chip Voltage Controlled Crystal Oscillator (VCXO)



Texas Instruments provides a portfolio of low-power, low-jitter, programmable clock generators capable of generating up to nine output clocks from a single input frequency. This level of functionality provides you with capabilities previously unavailable in clock/timing products.

Device	Supply Voltage (V)	I/O Voltage (V)	# of PLL	# of Outputs	Output Frequency (MHz)	Temperature Range (°C)	Package (TSSOP)
CDCE949	1.8	2.5/3.3	4	9	230	–40 to +85	24
CDCE937	1.8	2.5/3.3	3	7	230	–40 to +85	20
CDCE925	1.8	2.5/3.3	2	5	230	–40 to +85	16
CDCE913	1.8	2.5/3.3	1	3	230	–40 to +85	14
CDCEL949	1.8	1.8	4	9	230	–40 to +85	24
CDCEL937	1.8	1.8	3	7	230	–40 to +85	20
CDCEL925	1.8	1.8	2	5	230	–40 to +85	16
CDCEL913	1.8	1.8	1	3	230	–40 to +85	14



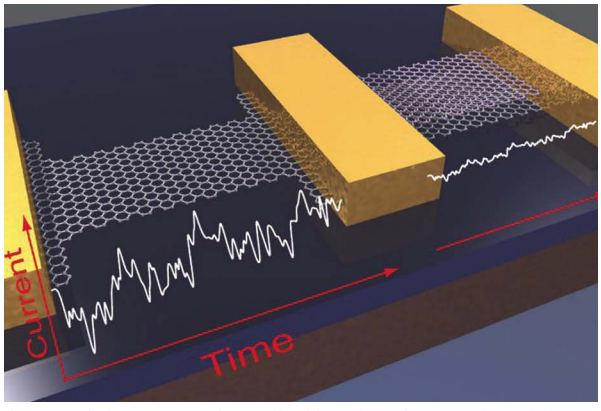
www.ti.com/clocks **1.800.477.8924 ext. 13971**
Get Samples and Evaluation Modules

Texas Instruments

Atomic-sized graphene has use in nanoelectronics

IBM researchers recently discovered that graphite may find use as a material for building nanoelectronic circuits smaller than those in today's silicon-based computer chips. The researchers have found a way to suppress unwanted interference of electrical signals that occur when shrinking graphene, which is a 2-D, single-atomic-layer-thick form of graphite, to dimensions of just a few atoms. Graphene is a honeycomb-like lattice of carbon atoms, similar to atomic-scale "chicken wire," which has attracted strong scientific and technological interest because it exhibits promising electrical properties and could find use in transistors and circuits at scales vastly smaller than components inside today's tiniest computer chips.

One problem in using these nanodevices is the inverse relationship between the size of the device and the amount of uncontrolled electrical noise that the devices generate. As they become smaller, the noise grows increasingly larger, and this effect occurs in traditional silicon-based devices as well as in graphene nanoribbons and carbon-nanotube devices. IBM researcher Phaedon Avouris, PhD, who leads IBM's exploration into carbon nanotubes and graphene, notes that the effect of noise becomes larger at the nanoscale because the dimensions approach the nearly smallest limits, down to only a handful of atoms, and the created noise can overwhelm the electrical signal. However, IBM scientists have found that they can suppress the noise in graphene-based semiconductor devices.



A second sheet of graphene significantly reduces noise, giving promise to this material's potential use in nanoelectronics.

> The strong electronic coupling between the two graphene layers inhibits the noise.

In experiments, IBM used a single layer of graphene to build a transistor and found that, as the device became smaller, noise increased. When they built the same device with two sheets of graphene instead of one, however, they were able to suppress the noise, and these bilayer graphene ribbons could prove useful for building future semiconductor devices for use in sensors, communications devices, computing systems, and more.

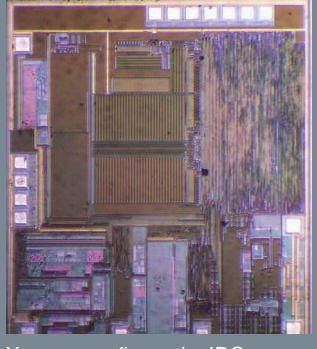
The strong electronic coupling between the two graphene layers inhibits the noise by counteracting the influence of the noise sources: The system acts as a noise insulator. Although further detailed analysis and studies are necessary to better understand these phenomena, the findings provide exciting opportunities for graphene bilayers in a variety of applications.

—by Ann Steffora Mutschler

▷**IBM Corp**, www.ibm.com.

SMART RFID CHIP AUTOMATES DATA-LOGGING, -TRACKING SYSTEMS

The passive/semipassive IDS-SL13A tag chip from IDS Microchip AG finds use in single-cell, battery-powered smart-RFID (radio-frequency-identification) labels. An external 1.5 or 3V battery powers the chip's integrated real-time clock and EEPROM for on-chip logging of data from the internal temperature sensor, accurate to 0.5°C, and external sensors through an analog-sensor interface and an ADC. An RFID reader accesses the chip through three-level password authentication. An SPI (serial-peripheral-interface) port supports external display circuitry, communication, control, and direct access to the internal EEPROM. The chip includes an alarm system and algorithms to calculate shelf life. The chip consumes a maximum of 3 μA in standby-logging mode and 300 μA during temperature measurement and data writes to EEPROM. The company estimates a one-year lifetime for an IDS-SL13A-based smart label with a 30-mAhr battery.


You can configure the IDS-SL13A for either battery-powered RFID tags or passive-system applications.

The IDS-SL13A also works in passive mode with no battery without the real-time-clock function in applications using an RFID reader to initiate data logging and storage. In the standby passive state, requiring no logging or measurement, the device consumes less than 100 nA.

IDS-SL13A chips are now available for sampling as tested wafers or packaged parts in 12-pin QFN packages and will be in full production in the third quarter of 2008. The price is less than €1, or approximately $1.60 (100,000).

—by Margery Conner

▶**IDS Microchip AG, www.ids-microchip.com.**

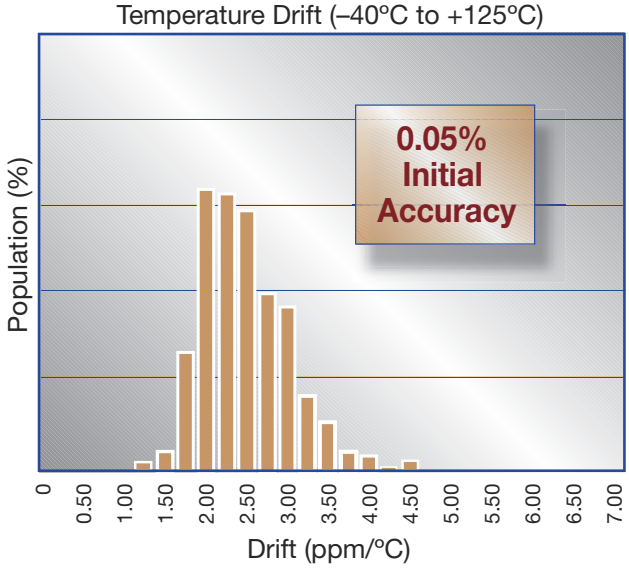
05.15.08

Precision Voltage Reference Families

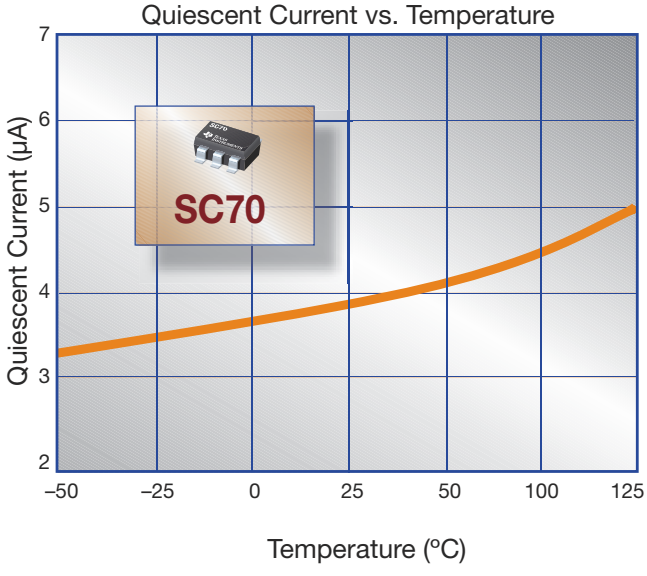
High Accuracy or Low Power

High-Performance Analog>>Your Way™

REF50xx



REF33xx



The new **REF50xx** and **REF33xx** voltage reference families from TI offer new levels of performance for high-accuracy industrial applications and precision, low-power applications. The REF50xx provides 3ppm/°C (max) drift, 0.05% accuracy and 3µVpp/V noise—an ideal combination for meeting the requirements of high-resolution, industrial ADCs. Featuring a low 5µA (max) quiescent current, the REF33xx has the ability to sink and source up 5mA output current and operates as low as 1.8V, making it ideal for portable applications.

Product	Accuracy (%)	Output (V)	Drift (ppm/°C) (max)	I_Q (µA) (typ)	Output Current (mA)	Package	Price (1k)*
REF50xx	0.05	2.048, 2.5, 3.0, 4.096, 4.5, 5	3	800	±10	MSOP-8*, SO-8	$3.50
REF50xxA	0.1	2.048, 2.5, 3.0, 4.096, 4.5, 5	8	800	±10	MSOP-8*, SO-8	$1.85
REF33xx	0.15	1.25, 1.8, 2.048, 2.5, 3.0, 3.3	30	3.9	±5	SC70, SOT23-3	$0.85
REF32xx	0.2	1.25, 2.048, 2.5, 3.0, 3.3, 4.096	7	100	±10	SOT23-6	$1.70
REF31xx	0.15	1.25, 2.048, 2.5, 3.0, 3.3, 4.096	15	100	±10	SOT23-3	$1.10
REF30xx	0.2	1.25, 2.048, 2.5, 3.0, 3.3, 4.096	50	42	25	SOT23-3	$0.60

** Suggested resale price in U.S. dollars in quantities of 1,000. *Available 2H 2008. New products are listed in **bold red**.*

www.ti.com/precisionreferences **1.800.477.8924 ext. 4463**
Get Data Sheets and Samples

Texas Instruments

Lossless coding comes to portables

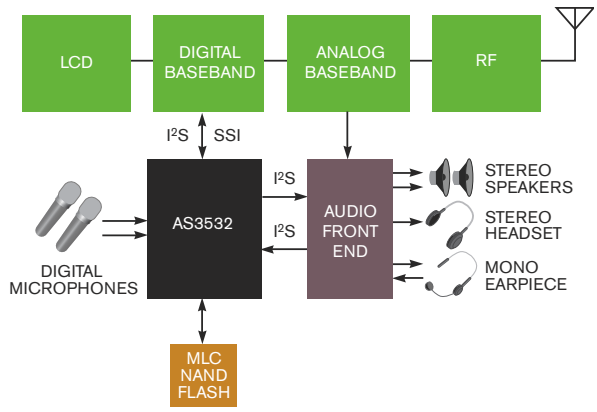
With more widespread use of MP3-player docking stations, consumers are increasingly finding that the sound quality from portable devices does not match that of CD sound, according to austriamicrosystems. Consequently, the company has introduced the AS3532 media-player IC that handles lossless-compression music content and operates within a 5-mW limit. The company aims to bridge the gap between the audio experience of music phones and high-fidelity home-audio devices.

Designers frequently base portable players on a processor core, such as an ARM (www.arm.com)—perhaps with a DSP core—that performs the MP3 decompression in software. Austriamicrosystems has retained an ARM core as a controller but has built an optimized hardware-audio engine to perform the decompression. According to Roberto Simmarano, the company's senior marketing director for the communications-business unit, when you move from a lossy codec to a lossless one, the amount of processing required from a programmable-DSP architecture rises sharply: More operations at a higher clock rate mean more power. Within its 5-mW power budget, the IC can process 24-bit content at a 192-kHz sample rate; many portable devices today are limited to 16-bit data at 44.1 or 48 kHz.

The audio engine executes the decompression and playback of most popular compressed audio formats, such as MP3, WMA (Windows Media Audio), and AAC (Advanced Audio Coding), for the least amount of power consumption with zero CPU load. The audio postprocessor implements an ASRC (asynchronous-sample-rate converter) with near-transparent quality. The processor achieves a range of 136 dB using a multipass algorithm, a multichannel mixer with limiting function, and a 10-band graphic equalizer. Three sets of I²S outputs can independently control stereo speakers, the associated subwoofer, and headphone or line outputs or can act as multichannel audio outputs. A digital microphone fills out the audio requirements for new-generation mobile phones. Interfaces that are part of the AS3532 can support either peer mode to a baseband-phone IC or a black-box companion-music subsystem. In this scenario, the IC provides direct support for a variety of removable and embedded flash-memory types. AMS supplies the chip in a 66-mm CT-BGA package. Simmarano declines to discuss pricing, as he is marketing this part directly to tier-1 and -2 phone handset makers; further related parts will address other sectors of the audio industry.

—by Graham Prophet

▷**austriamicrosystems**, www.austriamicrosystems.com



The AS3532 media-player IC handles lossless-compression music content and operates within a 5-mW limit.

CSR HITS $6 PARTS COST FOR DSP-BLUETOOTH HEADSET

In the world of Bluetooth-headset design, every cent of the BOM (bill of materials) counts. With that fact in mind, CSR has introduced single-chip devices with BOM figures of $5 and $6. The BlueVox2 headset costs $5, and the extra $1 adds DSP for active noise cancellation to remove ambient sounds from the microphone channel. The company's Kalimba block adds the DSP function, with either single-microphone operation or dual-microphone channels; the second microphone is for ambient noise and adds just a few cents to the cost. The DSP code is in ROM, also lowering costs.

CSR's new Bluetooth headset employs the company's AuriStream codec and costs as little as $5.

The chip operates to Bluetooth 2.1 EDR (enhanced data rate) and implements the company's AuriStream codec for improved voice quality and lower power when both ends of the link can use it or autonegotiates to fall back to a standard codec if not. Power management, including battery charging, is on-chip; the Bluetooth core is CSR's Bluecore5 block, and the control processor is an XAP2++ RISC core from Cambridge Consultants (www.cambridgeconsultants.com). A reference design is available; it includes not only complete layout and component information, but also a built and working example. Power demand is 11 to 14 mA at 3.7V, depending on the codec in use. Transmitter power is 8 dBm, and receiver sensitivity is −90 dBm. These figures provide greater link robustness and avoid cross-body signal-loss dropouts, according to the company. The non-DSP version has similar RF performance and power requirements of 6.5 to 8.5 mA.—by Graham Prophet

▶**CSR, www.csr.com.**

Our newest wireless infrastructure innovations

AD6655 IF Diversity Receiver
Reduces cost of deployment to allow more base stations to improve network quality. 3G support allows increased capability for high data rate applications.

AD9230 Single, 12-Bit 250 MSPS ADC
Better base station power efficiency using digital predistortion techniques reduces electricity demand and provides better spectrum purity.

AD9788 Dual, 16-Bit 800 MSPS Transmit DAC
Simplifies transmit architecture by eliminating mixing stages and provides best ACLR for enhanced network performance.

AD8375 and AD8376 Variable Gain Amplifiers
These VGAs enable excellent dynamic range to capture faint transmitted signals in the presence of strong signals.

AD9549 and AD9516 Dual Input Network Clock Generator and Distribution Function
Very low noise clock sources ensure best signal quality across multiple wireless platforms.

Quality connections—in less space, using less power—that's why more base station engineers speak to Analog Devices

As fast as wireless connectivity became pervasive, Analog Devices data converters became the preferred signal processing standard within base station designs. Today, that data conversion technology is just part of a growing family of analog, digital, RF, and mixed-signal solutions for flexible, software-based radio architectures that support wireless standards from GSM to WiMAX. ADI continues to leverage more than 40 years of signal processing innovation to reduce the size, cost, and power demands of base stations, while enabling increased data rates and delivering the calling experience wireless users prefer. And we offer the same application-tuned advantages for medical, industrial, consumer, and automotive designs.

To experience what Analog Devices can do for wireless infrastructure and for other signal processing designs, call 1-800-AnalogD or visit *www.analog.com/basestation*.

analog is everywhere.™

www.analog.com/basestation

ANALOG DEVICES

VOICES

Intellon's Mark Hazen on the HomePlug AV powerline-networking alternative

Last fall, powerline-networking provider DS2 weighed in with its thoughts on the technology's strengths, shortcomings, and future directions (see "Voices: Chano Gómez on powerline networking's 'universal' hope," *EDN*, Dec 14, 2007, pg 18, www.edn.com/article/CA6512163). In this follow-up interview, Senior Marketing Communications Engineer Mark E Hazen, from HomePlug AV (audio/video) consortium representative Intellon, DS2's primary competitor, shares his perspectives on a similar set of questions. Read an extended version of this interview at www.edn.com/080515voices.

How do HomePlug technology's attributes enable it to coexist, supplement, or supplant other traditional data-distribution technologies for both LAN and WAN applications now and in the future?

A Great question. HomePlug technology is playing a strong support role both inside (LAN) and outside (WAN) the home. Because of HomePlug's attributes, such as whole-house coverage, noise immunity, a standards-based approach, secure communications, and multivendor support, operators view it as a network 'backbone' technology, not supplanting other forms of home networking but instead providing a means to work in concert with other networking technologies such as Wi-Fi. In fact, multiple HomePlug-Wi-Fi-bridge products are currently in the market, which allow consumers to expand their coverage simply by plugging in a bridge anywhere in their house where Wi-Fi coverage is weak or nonexistent. It is the value of HomePlug as this 'bridgeable technology' that contributes to its growing popularity.

HomePlug PLC-LAN technology supports any to-the-home WAN technology and actually provides much higher speeds throughout the home than most services to the home. As a WAN technology, HomePlug is starting to see some growth, especially in areas of the world that are underserved by xDSL [digital-subscriber line] or cable Internet. BPL [broadband-over-powerline] access can provide typical broadband service to the home through the medium-voltage lines across the neighborhood and into the low-voltage service lines feeding the home. In this way, a utility can participate and compete in the broadband-services industry, in the same way a telephone-company, MSO [multiple-switch-operator], satellite, or WiMax [worldwide-interoperability-for-microwave-access] provider might.

HomePlug AV is specified as a '200-Mbps' technology, but testing results suggest that it delivers only a limited percentage of that speed in real-life usage environments. How do you address potential consumer confusion and frustration, when they don't get the performance results that the '200-Mbps' stamp on the product box might otherwise suggest they'll achieve?

A This is another great question. There is some confusion about this [situation] in all data-communications communities, including wireless ones. Take, for example, IEEE 802.11g Wi-Fi, which is known as a 54-Mbps technology; 54 Mbps is the PHY [physical]-medium rate minus forward-error-correction bits. The standards bodies, during technology and specification development, decide which type of PHY rate they will associate with their standard. In the case of 802.11g, 54 Mbps is the coded PHY rate, as opposed to the higher raw PHY rate [which is slightly higher than 70 Mbps]. Few consumers are aware of this distinction. Even so, it allows the Wi-Fi-standards people to churn out different standards classes with the same apples-for-apples PHY rating.

Regarding HomePlug AV, 200 Mbps is the raw PHY rate, which includes forward-error-correction bits. This approach follows that of the wireless technologies—that is, associating a PHY rate with each wireless standard. Some of our customers who market in retail state on their boxes what UDP [User Datagram Protocol] and TCP [Transmission Control Protocol] rates consumers should expect.

The UDP is the fastest MAC [medium-access-control] protocol, because it does not require acknowledgments to each packet sent. It finds use for streaming music and video, and for VOIP [voice-over-Internet Protocol] telephony. Our tests have shown that HomePlug AV typically delivers a UDP rate across the home in the 50- to 90-Mbps range, depending on noise and attenuation.

The TCP is slower than UDP but is more careful, checking to make sure that each packet was successfully received and, if necessary, repeating the transmission. HomePlug AV typically delivers a TCP rate across the home in the 30- to 60-plus-Mbps range, depending on noise and attenuation.

A protocol that many use to judge the performance of a digital technology is Windows File Transfer. This protocol runs under TCP and is therefore even slower than TCP. The peak Windows File Transfer throughput for HomePlug AV is around 36 Mbps.

It is important to understand that, whether the technology is wired or wireless, this hierarchy of protocol performance is always true.

We need more editors to understand this [fact] to help us educate the public. Thanks for asking the question in this forum.**—by Brian Dipert**

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Hysteresis Blocks Magic

Q. Can I recalibrate my precision analog circuits to achieve higher accuracy?

A. There is no magic[1] process for upgrading the precision of analog circuitry. A phenomenon known as hysteresis limits just how repeatable it can be.

After time, the most common electronic measurement is of temperature. Temperature sensors use a number of technologies, but the simplest and least expensive ones measure the difference in voltage between two PN junctions operating at differing current densities or the change in voltage in a single junction as its current density is varied. This voltage is proportional to the absolute (Kelvin) temperature of the junction.

Low-cost temperature sensors have an accuracy of two or three degrees Celsius, whereas the best ones are accurate to about half a degree. It is quite common for users to try to calibrate such sensors to achieve greater accuracy.

Up to a point, such calibration is possible (but quite expensive, which is why such devices are not routinely manufactured), but it is not possible to calibrate to any arbitrary degree of accuracy.

Suppose that, using a magic thermometer and voltmeter, we measure the temperature and output of a semiconductor sensor with infinite accuracy. Then, after heating and cooling the sensor, we re-measure the output, at exactly the same temperature, and find that the output is slightly different. Repeated measurements yield results with a Gaussian distribution about a mean value.

The mechanism causing this variation is known as thermal hysteresis. It arises from thermo/mechanical stress in the integrated circuit. Silicon chips are made with a very complex pattern of silicon, silica (silicon dioxide - SiO_2), aluminium, copper, and a variety of other materials, each of which has a different coefficient of thermal expansion. Each time the chip's temperature is changed, the stress pattern due to differential expansion/contraction will change too. The structure is complex, making many different stress patterns equally likely. Stress in conductors changes their resistance, causing small changes in the circuit's calibration.

It is therefore impossible to recalibrate a temperature sensor to much higher accuracy simply by measuring its response very accurately. The best that can be achieved with available sensors is on the order of 0.1°C. If we made a much larger chip the stress effects would average out over the larger area, but a useful improvement would require a very large and expensive chip. Similar effects are seen in other precision analog ICs, especially voltage references, but, as with temperature sensors, they rarely become large enough to affect the published specifications. If you look for them with sufficiently accurate test gear, however, you will certainly find them.

[1] *(Arthur C.) Clarke's Third Law states that "Any sufficiently advanced technology is indistinguishable from magic."*

To learn more about Hysteresis

Go to: http://rbi.ims.ca/5711-101

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

raq@reedbusiness.com

For Analog Devices' Technical Support, Call 800-AnalogD

BY BONNIE BAKER

RMS and peak-to-peak noise trade-off

Have you ever noticed that random noise has a predictable pattern? Nature duplicates this pattern in many ways—the gene pool, gambling, and even my driving "habits."

There are two ways to describe random analog noise. The first uses the standard deviation of a collection of converter digital-output samples. The data's standard deviation is equal to the rms (root-mean-square) value. The second uses the standard deviation and a constant crest factor to describe a converter's noise with a peak-to-peak value. Specifications with rms or peak-to-peak descriptors use statistical methods to arrive at a single number that describes the analog device's noise behavior or an ADC.

You can use rms to describe the system's noise power. "RMS" may appear with the specified units, or it may be implied. Usually, a noise specification includes the rms term. However, an SNR (signal-to-noise-ratio) specification doesn't. SNR uses only decibels for units.

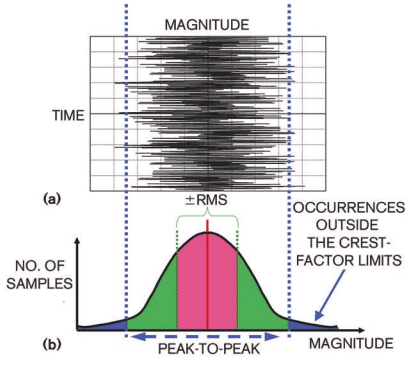


Figure 1 Organize data from a time plot (a) into a histogram to help determine rms and peak-to-peak limits (b).

When describing noise with an rms number, you are referring to the positive and negative range of the data's standard deviation. Although the noise's rms value from a converter is well-defined, you can predict the instantaneous position on the X axis only with the theory of probability. It is possible to create a histogram plot from the dc-output data (**Figure 1a**). By collecting more than 1000 data points, this histogram approaches the shape of a gaussian distribution, or bell-shaped curve. The two standard-deviation or rms lines capture a significant number of the noise occurrences. The probability that the noise from an analog device produces one output value that lands between the two rms lines is approximately 68%.

If you are putting output data from an ADC into a digital display, the peak-to-peak noise representation becomes important. Here, you determine how often and how many display digits can fluctuate, keeping in mind that fluctuating digits create user or customer insecurity. With a histogram plot, the rms limits exclude a considerable amount of data (**Figure 1b**). Multiplying the doubled standard deviation by a crest factor expands the percentage of occurrences underneath the curve. The crest factor for noise occurrences is a statistical estimate that determines the probability that an occurrence of a noisy event will remain within a defined boundary.

TABLE 1 DISPLAY FLUCTUATION

Crest factor	Occurrences inside limits (%)
2.6	99
3.3	99.9*
3.9	99.99
4.4	99.999**
4.9	99.9999

*Industry standard
**Stable to five display digits

Predicting the allowable fluctuation in your data display is relatively simple. After choosing a crest factor, multiply the value of two standard deviations by the selected crest factor. The industry standard is 3.3, which is appropriate for a three-digit display (**Table 1**). If you are keeping a five-digit display stable, use a crest factor of 4.4. The lower digits in your display will fluctuate 0.001% of the time.

Use rms or peak-to-peak figures to describe an analog device's input- or output-referred noise. Data sheets and labels may have noise specifications with units such as volts rms or volts peak-to-peak. You can quickly describe the noise power visible at the output of a converter with the data's standard deviation. Control the fluctuating digits in your display by defining peak-to-peak limits. EDN

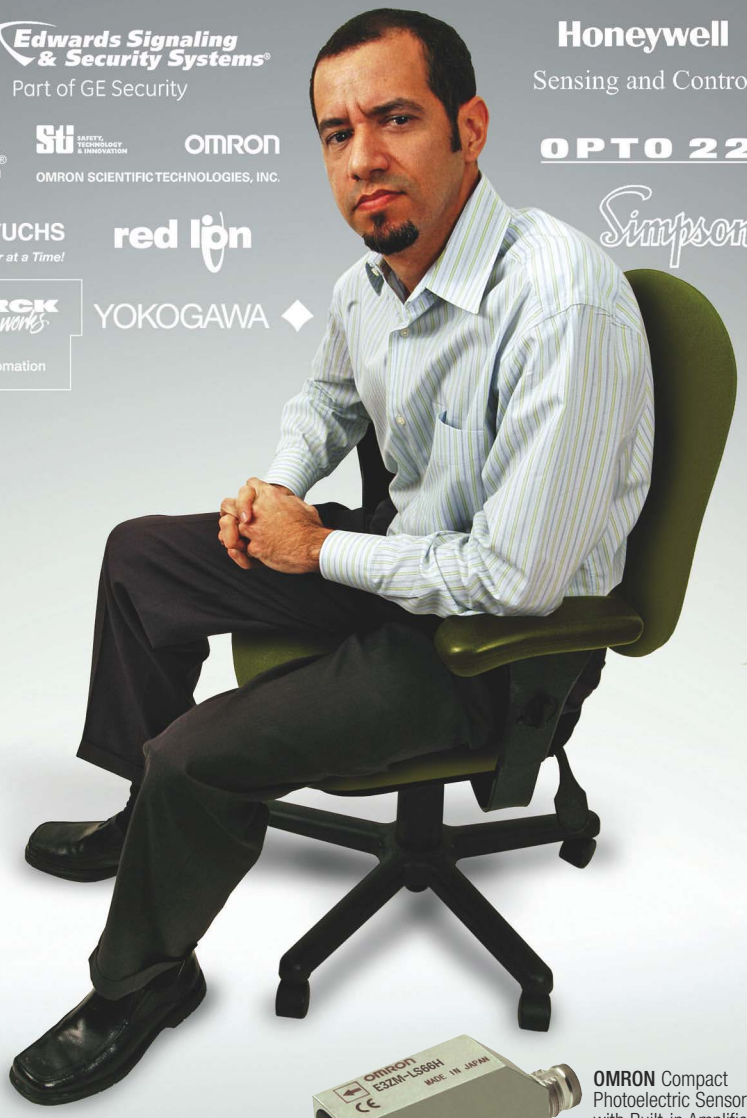
Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

MORE AT EDN.COM

Go to www.edn.com/080515bb and click on Feedback Loop to post a comment on this column.

Design with the best: Automation

BANNER® more sensors, more solutions
BRAD HARRISON From Daniel Woodhead Company
CARLO GAVAZZI Automation Components
Crouzet More than a standard
crydom
EATON Cutler-Hammer
DANAHER INDUSTRIAL CONTROLS
Edwards Signaling & Security Systems® Part of GE Security
Honeywell Sensing and Control
IDEC
MACROMATIC
OMRON® INDUSTRIAL AUTOMATION
STI SAFETY, TECHNOLOGY & INNOVATION
OMRON SCIENTIFIC TECHNOLOGIES, INC.
OPTO 22
Panasonic
Panasonic Electric Works Corporation of America
PEPPERL+FUCHS Building Trust...One Sensor at a Time!
red lion
Simpson®
SQUARE D Schneider Electric
Telemecanique™
TURCK Industrial Automation
YOKOGAWA



"Live chat with tech support.
That's important.

Dependable delivery.
That's important, too.

The best selection of sensors.
That's critical."

OMRON Compact Photoelectric Sensor with Built-in Amplifier
22M3779

Design with the best brands

You'll find the best components and the best information in one site. Visit www.newark.com/motion to see the latest advances in automation from world-class suppliers.

Find more at www.newark.com and 1.800.4.NEWARK

Supplier Authorized Distributor

Newark™
DESIGN WITH THE BEST

A Premier Farnell Company

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Third-party-IP providers: physical-design questions, part one

As this column has discussed previously, selecting an IP (intellectual-property) provider involves several technical and business issues. On the technical front, the additional levels of selection complexity involve the physical-design view of the IP. The issues that follow assume that the IP under consideration meets the design and performance specification and targets the correct process-technology option. In addition to your architectural and performance goals, six categories of the physical view should be part of the selection criteria for the IP: block pins and grid, blockages and overlayer routing, power supplies, global signals, placement and rotation, and embedded blocks and clocks.

You should have a good understanding of the first category—block pins and grid—as it's been around for more than 30 years. The most important aspect to understand is that a design will support multiple simultaneous grids that all relate to different functions and criteria during the design. All of these grids should be related integral multiples of at least one of the other grids.

The minimum grid is the database resolution. Next come the mask-fracture/e-beam-spot-size resolution, the minimum drawn data (digitizing) grid, the routing grids, and the cell-placement grid; none of these values is the same as the minimum database-resolution grid value.

Process geometries that exceed one wavelength require only simple MDP (mask-data prep), DFM (design for manufacturing), and OPC (optical-proximity correction). These options can support wire jogs that come from nonaligned or off-grid pins and wires. In these processes, connectivity is the main driver, and you can use standard subgrid routers, which simply allow DRC-clean wiring by shifting wires to the digitizing grids from the X- and Y-direction router-grid values.

In such simple cases, you can make off-grid pins and connections anywhere on the line without major consequences. In subwavelength processes, however, connections need to be clean, with no overhang and preferably all in the same direction. Otherwise, the DFM and OPC create context-specific options that are data-intensive and impact reliability. **Figure 1** depicts examples of these cases.

Select physical IP with the manufacturability of the block in mind. It is inappropriate to use IP created with both X and Y routing-grid pitches that differ from the pitches your SOC (system-on-chip) assembly uses. If the IP is incompatible with your flow, ask the provider to change the PHY (physical)-layer view so it aligns with your flow, change the technology files and grid structures of the place-and-route environment and for the whole SOC, or choose another IP-block/provider. Never modify the IP yourself; you can't be sure of the impact of your changes.

As for the pins themselves, there are several basic criteria that the plethora of new IP providers is leaving behind: Any part of the IP block that connects at a level of hierarchy above the block must have a pin; all pins in the layout should appear in the netlist views; all pins in the netlist should appear in the layout view; and the power-supply pins must have names that identify the correct operating-voltage rail. The last issue is a new pin-naming criterion that arose from the various power-reduction and multivoltage-operation techniques. EDN

Contact me at pallabc@siliconmap.net.

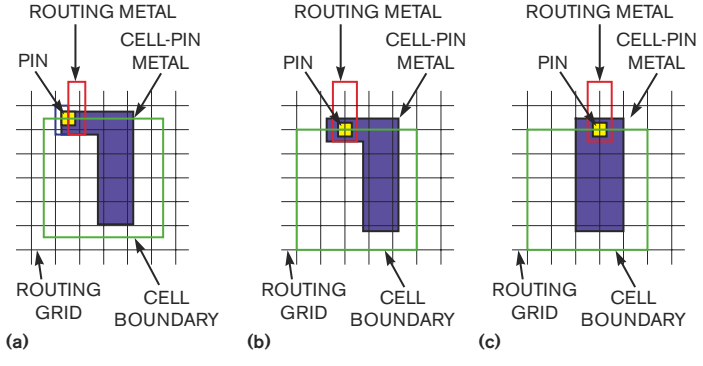


Figure 1 You can make off-grid pins and connections anywhere on the line without major consequences (a). In subwavelength processes, connections must be on-grid with no overhang (b and c).

Pick a waveform

Any waveform

Agilent 33220A/33250A
Function and Arbitrary Waveform Generator

FREE
Arbitrary Waveform Library
www.agilent.com/find/any_wave

If you see a function generator in use today, the odds are it's an Agilent. Why is Agilent the best-seller?

Versatility. Our generators produce the most powerful array of waveforms in the industry. They include all the functions you'd expect, with pulse and arbitrary waves of up to 64k points—accurate, stable, low noise. And the 33220A is the first arb function generator designated LXI compliant.

Right now, you can get our Arbitrary Waveform Library absolutely free. The library includes 20+ waveforms that can be used immediately or modified to suit your own applications.

It's your deal. Call today to learn more, or visit us at
www.agilent.com/find/any_wave

Agilent Authorized Distributor

METRICTEST™
6,000 instruments. One source.

866-436-0887 www.metrictest.com/agilent

Agilent Technologies

PRY FURTHER AT EDN.COM
Go to www.edn.com/pryingeyes for past Prying Eyes write-ups.

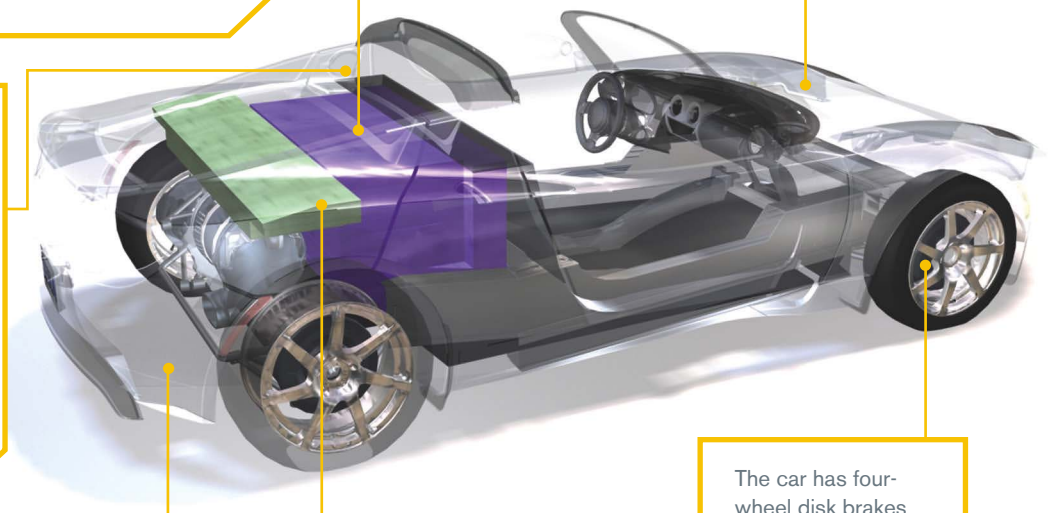
The Tesla Roadster: sporty *and* electric

A MODERN ELECTRIC SPORTS CAR PRESENTS A UNIQUE DESIGN CHALLENGE.

The enabling technology for the Tesla Roadster is the lithium-ion battery. The RC-modeling community years ago discovered that lithium-chemistry batteries created fast, light, quiet, and quickly rechargeable planes, so you can see why the technology first found use in model aircraft. Automotive design has all the challenges of aircraft design, along with the more brutal constraint of lower cost. Tesla (www.teslamotors.com) wisely chose to design a $120,000 sports car rather than a family sedan or economy box. This choice gave it the freedom to use the latest technology to make a viable vehicle.

The Roadster initially used 6800 lithium-ion, 18×65-mm laptop-computer batteries. Cell-balancing and safety concerns may require the use of ferric-anode-lithium chemistry from A123 (a123systems.com). This technique would use larger cells to reduce the cell-count and ferric chemistry to prevent thermal runaway.

Although the air-conditioning unit cools the passenger compartment, its primary task is to cool the battery pack, so the Environmental Protection Agency's rules requiring air conditioning to run during mileage tests don't impact the car.

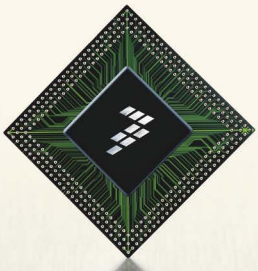


The car's charger port charges in approximately 3.5 hours and gives a range of 220 miles. If Tesla switches to ferric-anode lithium-ion batteries, charging may be more aggressive, but the vehicle's range may suffer due to lower energy density of ferric-anode chemistry.

Tesla made extensive use of carbon fiber and fiberglass in the vehicle's body to get the car's curb weight down to 2700 lbs. Low weight is critical to making a viable electric vehicle. About 20% of the car's parts come from Lotus.

The vehicle uses a flux-vector inverter, and multiple DSPs create the three-phase sine waves and provide regeneration current to recharge the battery while a driver is braking.

The car has four-wheel disk brakes with an antilock-braking system and forged-alloy wheels. An electric vacuum pump provides power assistance.



It's the best connected 15-year-old in the MCU industry.

ColdFire® Architecture. The perfect 32-bit compilation.

The ColdFire Architecture has a 15-year heritage steeped in innovation. With more than 100 individual devices, ColdFire has one of the broadest 32-bit portfolios in the industry. Whether it's USB, Ethernet, CAN or ZigBee,® ColdFire connects and controls millions of networked products in homes, offices and factories around the world. ColdFire also enables your design to keep pace with today's eco-trends thanks to its industry-leading, ultra-low-power 32-bit MCU. And to make its own ecosystem even stronger and more vibrant, we are now openly licensing ColdFire V1. Find out what ColdFire can do for you.

Meet ColdFire at freescale.com/coldfire101 and save 50% on the JM Low-Cost Demo Kit*.

freescale™ semiconductor

* While supplies last.

See farther down the road than ever before.

Avoid risks with SoC "*Virtual Prototyping*" before design start.

Toshiba innovation now enables SoC customers to view a "Virtual Prototype" before design start...with chip, package and PCB constraints...long before conventional prototypes are available. This dramatically minimizes risks, cuts costs and can reduce time-to-market by months. Toshiba's bold new capability further cements its leadership as an EDA/design powerhouse for ASICs 65nm and beyond. In addition, our one-stop-shop model offers the flexibility of handoff from RTL to GDSII. For your next SoC project, look no further than Toshiba, one of the world's largest SoC/ASIC producers, and see farther down the road to success than ever before.

Play the ChipQuest On-line Game to win a Noise Cancellation Headset, Wireless Internet Hot Spot Finder, or high-powered flexible LED light, (while supplies last), plus all players will be entered in monthly drawings to win a Garmin GPS nuvi 200. Enter at SoCworld.toshiba.com.*

*Qualified Engineers only

Analog Applications Journal

DESIGN BRIEF

Driving a WLED Does Not Always Require 4 V

By Will Hadden
Power Management Products, Portable Power DC/DC Applications

Featured in the latest online issue

- Using a touch-screen controller's auxiliary inputs
- Driving a WLED does not always require 4 V
- Host-side gas-gauge-system design considerations for single-cell handheld applications
- Using a buck converter in an inverting buck-boost topology
- Download your copy now at **www.ti.com/aaj**

The popularity of white-light-emitting diodes (WLEDs) has skyrocketed, primarily because they are used to provide backlight to portable electronics displays. The common belief is that a single WLED requires a 4-V drive voltage. Since a Li-ion battery provides an average voltage of 3.6 V, the general industry consensus is that a step-up converter is required to power WLEDs from a single-cell Li-ion battery. As a result, many ICs are available for driving WLEDs, most requiring an external inductor or flying capacitors to boost the cell voltage high enough. As WLED technology continues to mature, the forward-voltage requirements continue to drop. Currently, there are many LEDs available with typical forward voltages (V_F) in the 3.2- to 3.5-V range with maximum ratings at 3.7 to 4 V. The datasheets usually specify these voltages at LED currents of around 15 to 25 mA. This abbreviated article discusses lower-current applications and how they affect the forward voltage of the WLED. It also introduces the TI TPS75105, a new LED driver designed to efficiently drive these lower-voltage LEDs with a reduced solution size and cost.

LED Forward Voltage

The WLED is similar to other standard p-n junction diodes. It does not conduct current until a sufficient forward voltage has been applied. After the threshold is exceeded, the forward current increases with the forward voltage of the WLED. A typical I-V curve for a WLED is shown in Figure 1.

Utilizing this graph is a simple task. As with typical diode I-V curves, the current rises sharply with the voltage after crossing the threshold. The typical forward voltage for the device in Figure 1 is specified to be 3.2 V at 20-mA forward current with a maximum of 3.7 V over process and temperature variations. This leads to the conclusion that the application requires a step-up DC/DC converter to properly drive the WLED from a single Li-ion cell with an output of 3 to 4.2 V. However, this is not necessarily the case. Take, for example, a 5-mA WLED-current application. The curve in Figure 1 shows that the forward voltage required to drive 5 mA is around 2.9 V, which is much less than the typical voltage required to drive 20 mA as specified in the datasheet. A boost converter is not required to drive a 2.9-V output from a 3.6-V Li-ion cell.

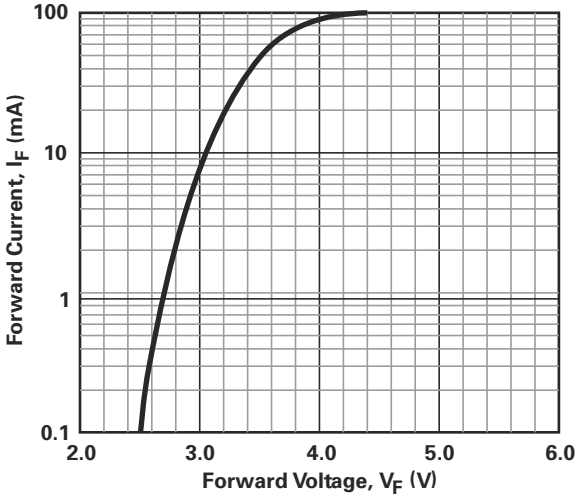


Figure 1. Typical WLED I-V curve[1]

WLEDs are specified with a typical value as well as a maximum value to cover lot-to-lot process and manufacturing variations. The I-V curves provided in the datasheet are usually specified with a part that falls at the typical specification. Although the curve shape is valid for every part that is manufactured, the curve shifts to the right or left depending on the forward voltage at the test conditions for that device. If we use another LED with the same part number as in the previous example, the forward voltage measures 3.7 V (the maximum rating) at the typical test conditions (20-mA forward current). This voltage, which is 0.5 V higher than a typical device, translates to a maximum forward voltage of 3.4 V (2.9 V + 0.5 V) required to drive this WLED at 5 mA. Depending on the cutoff voltage of the application, a boost converter is not needed to drive this particular WLED at 5 mA. This technique makes it easy to determine the maximum forward voltage for any application.

A Small LED-Driver Solution

A simple and lower-cost driver for low-current WLED applications is the ultrasmall TPS75105 LED driver IC. The TPS75105, a linear current source with an ultralow 28-mV dropout voltage, is used for driving four parallel WLEDs in two separate banks. This device provides four 2%-matched current paths in two separately enabled banks. The device is available in a 9-ball, 1.5-mm^2 wafer-chip-scale package (WCSP), requires no external components when using the default current output, and therefore results in a 1.5-mm^2 solution size. The application circuit for the TPS75105 is shown in Figure 2.

At first glance, using a low-dropout linear circuit to drive LEDs may seem impractical, given the linear regulator's reputation for low efficiency. However, the

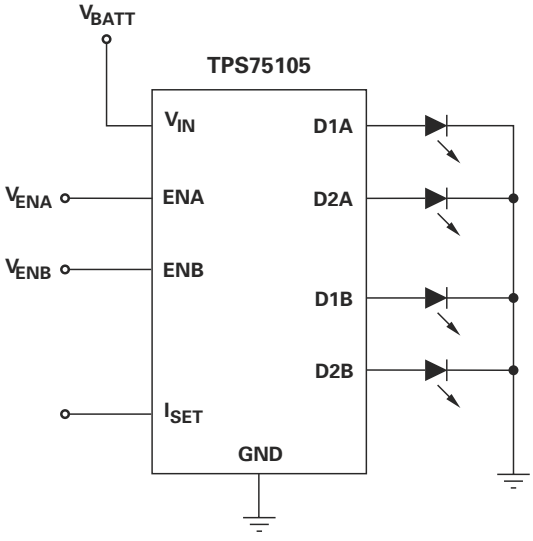


Figure 2. TPS75105 application circuit

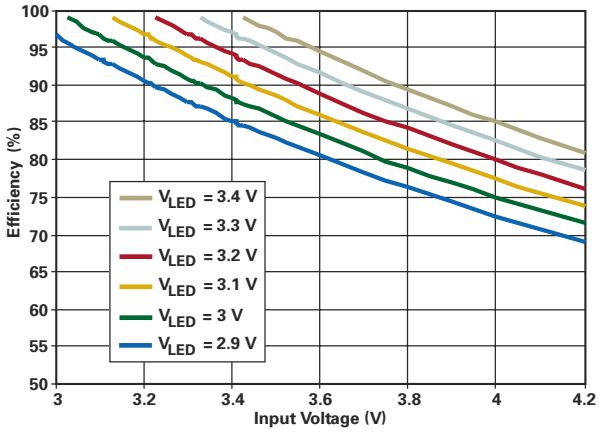


Figure 3. TPS75105 LED efficiency

efficiency of LDOs is often misunderstood. LDO efficiency is entirely based on the input/output voltage ratio; therefore, the efficiency of driving WLEDs can be quite high. For example, driving a 3-V WLED from a 3.6-V Li-ion battery input translates into an LED efficiency of 83%. Figure 3 shows the TPS75105 efficiency data for several different WLED forward voltages over the Li-ion battery range. The LED efficiency for the TPS75105 is comparable to or better than that of other WLED-driver solutions.

Conclusion

When an LED-driver application is evaluated, special consideration should be given to how much current the application requires. If it is well below the current at which the application's WLED V_F is specified, the WLED datasheet I-V curves should be reviewed to determine the actual V_F in the application. The application may be able to use a low-dropout linear current source such as the TPS75105 to achieve a small solution size and low cost without sacrificing the efficiency of a switching step-up converter.

Please see Reference 2 for the complete version of this article, which provides additional WLED information, a discussion about temperature variations, and an example showing LED efficiency of the TPS7510x over the Li-ion discharge curve.

References

1. Kingbright Corporation, City of Industry, CA, AA3528RWC/A Datasheet, Spec. No. DSAG3655.
2. View the complete article at http://www-s.ti.com/sc/techlit/slyt284
3. "Low Dropout, Two-Bank LED Driver with PWM Brightness Control," TPS7510x Datasheet (sbvs080)
4. TPS75105EVM User's Guide (slvu182)

As we approach the pervasive-computing era in which users will have round-the-clock access to information and services from any location, embedded-system designers are under growing pressure to boost the availability of servers, remote devices, and the data-transport infrastructure. Due to their application, embedded devices have a much higher reliability expectation than most other computing systems. You cannot stop or reboot some of these systems, such as those in critical applications, without risking loss of life, property, or essential information. In meeting these requirements, embedded-system designers use an arsenal of clever hardware- and software-redundancy techniques to routinely achieve availabilities as high as 99.999%, or less than six minutes of downtime per year.

"High availability" describes the characteristics of a system that allow it to sustain continuous operation in the event of hardware or software failures. With built-in monitoring and duplicate datapaths, a highly available system survives failures by transparently substituting alternative hardware or software components to reproduce normal functions. In general, a high-availability system also includes provisions for replacing failed components or upgrading performance without disrupting operation. With the advent of universal connectivity, data security also becomes an element of availability, because expected functions can see interruption due to an unauthorized hacker, malicious

ALWAYS ON: EMBEDDING HIGH AVAILABILITY

BY WARREN WEBB • TECHNICAL EDITOR

DESIGNERS ARE TUNING HIGH-AVAILABILITY ARCHITECTURES TO MEET CUSTOMER DEMANDS FOR A PERSISTENT DATA INTERFACE FOR THE NEXT GENERATION OF ULTRARELIABLE EMBEDDED-SYSTEM APPLICATIONS.

Figure 1
Adlink's aTCA-6900 features two quad-core Intel Xeon processors and dual mezzanine-card bays to extend the performance of high-availability AdvancedTCA systems.

software, or an external denial-of-service attack. Availability is normally defined as MTBF/(MTBF+MTTR), where MTBF is the mean time between failures and MTTR is the mean time to repair.

Although high availability has become essential to a growing list of embedded-system applications, escalading technology trends make the system-design task increasingly difficult. For example, as customers demand more functions in embedded devices, the added hardware and software components create new failure modes to anticipate. Obviously, added components work against higher availability and even generate other redundancies that continue to increase system complexity. The current movement toward ubiquitous connectivity also creates a host of data-security and communications-reliability problems for the high-availability-embedded-system designer. Although the most reliable system is probably a simple, stand-alone device with limited resources, designers must adapt a strategy that extends the availability of any embedded configuration.

AT A GLANCE

- High-speed serial-data links and switched-fabric technology enable dynamic paths so that you can reroute information around inoperable subsystems.
- Management software automatically monitors system operation and substitutes redundant components in the event of a failure or degraded performance.
- Hot-swap features enable repairs and upgrades with no downtime and pave the way for fault-tolerant, self-healing systems.
- Clusters of blade computers enable scalable, high-density, highly available server systems at reduced acquisition and operating cost.

CAN YOU HEAR ME NOW?

Most of the current tricks and techniques for extending service availability originated in the telecommunications industry. Over the years, telecom-equipment manufacturers devised multiple schemes to provide uninterrupted service despite hardware and software failures. Unfortunately, most of these schemes were proprietary, expensive to maintain, and difficult to update as requirements evolved. They also required long development cycles. Equipment designers were unable to use COTS (commercial off-the-shelf) building blocks, because there were no common built-in provisions for extending service availability. To tackle the availability conundrum, board manufacturers created a series of hardware and software specifications that could match the performance of proprietary systems.

One of the earliest standards to address availability was the IPMI (Intelligent Platform Management Interface) specification, which Dell, Intel, Hewlett-Packard, and NEC defined to allow local and remote monitoring of equipment for power management, cooling, electronic keying, and hot-swap transactions. IPMI interacts with a management controller that works on its own if the host processor is defective. With platform management, operators can monitor equipment for marginal operation or potential problems and correct them before they become system failures. PICMG (Peripheral Component Interconnect Industrial Computer Manufacturers Group) incorporated variations of IPMI into both the CompactPCI and ATCA (Advanced Telecom Computing Architecture) board-level specifications.

To derive the maximum benefit from IPMI, equipment customers needed a hot-swap capability to replace defective boards without shutting down their systems. Hot-swap systems require hardware and software that can dynamically route signals around defective components while waiting for repairs. One of the essential technologies of hot swapping is the physical connection between the board and the backplane. A simple direct connection can disrupt the other boards on the bus without controlling power-supply inrush current and backplane-signal connections. For example, CompactPCI uses staged pins of different lengths to control the physical connection to the backplane. Card guides ensure that board insertion is perpendicular to the backplane. The longer pins are the first to mate and supply power and ground to precharge the PCI-bus signals. Series resistance limits the power-supply current surge. The medium-length pins connect to the PCI-bus signals that are in a precharged, high-impedance, or disabled state. The shortest pins enable bus communications.

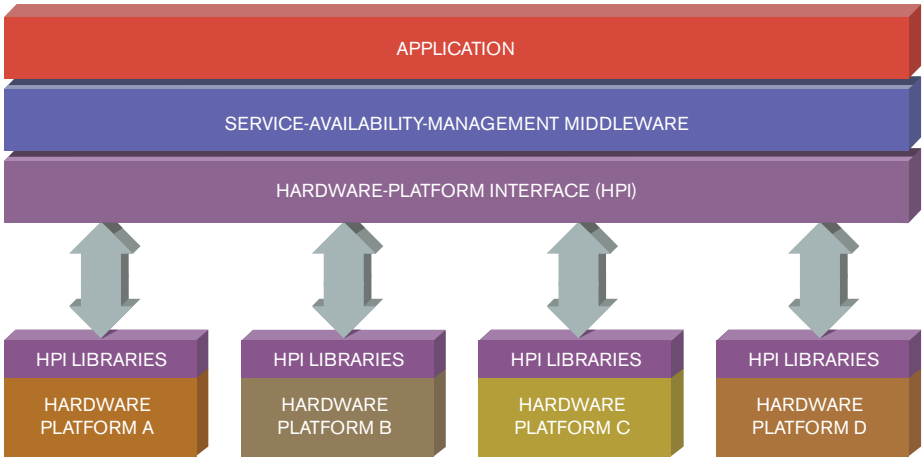


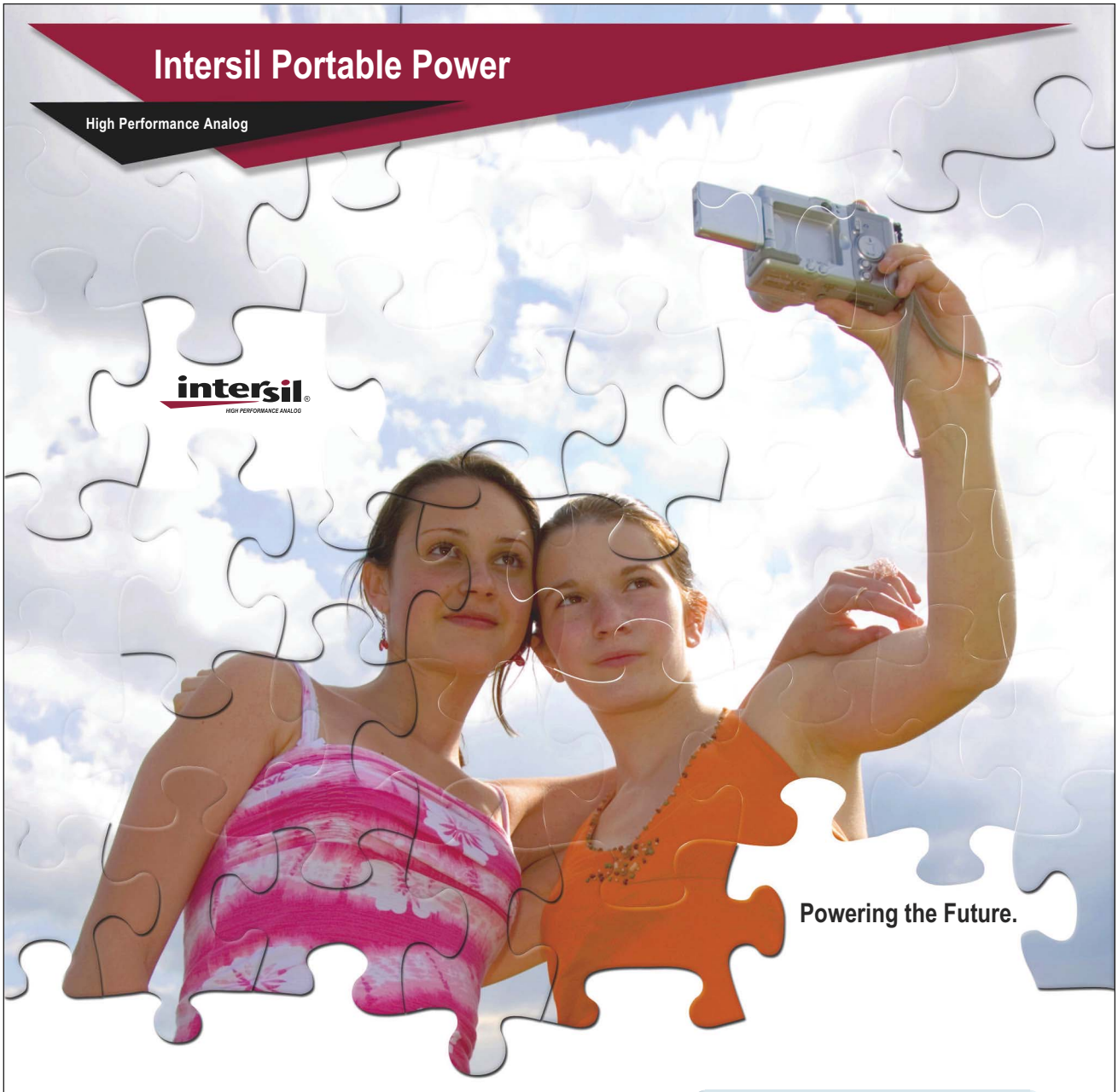
Figure 2 The hardware-platform-interface specification from the Service Availability Forum defines an interface between COTS hardware and management middleware.

FAILPROOF FABRIC

Serial-switched-fabric technology is another design innovation that has multiple benefits for high-availability systems. These architectures allow dynamic datapaths between computing nodes and support multiple simultaneous data transfers. A major benefit of a switched fabric is that each connection is a direct point-to-

Intersil Portable Power

High Performance Analog



Power your handheld devices with Intersil's high performance Power ICs.

Intersil's Portable Power solutions provide the management stability and design flexibility today's changing devices require.

Intersil Portable Power Management:

- Battery Chargers
- Overvoltage Protection
- Overcurrent Protection
- Battery Authentication
- LCD Display Power
- Low Drop Outs (LDOs)
- LED Backlighting
- Fuel Gauges
- Core Power
- DDR Power

Go to **www.intersil.com** for samples, datasheets and support

Intersil – Switching Regulators for precise power delivery.

intersil®
HIGH PERFORMANCE ANALOG

THE HIGH AVAILABILITY LINUX PROJECT HOSTS AN OPEN-SOURCE-DEVELOPMENT EFFORT TO PROVIDE A CLUSTERING ARCHITECTURE FOR THE LINUX OPERATING SYSTEM TO PROMOTE RELIABILITY, AVAILABILITY, AND SERVICEABILITY.

point datapath and yields better electrical characteristics, allowing higher frequencies and bandwidth than bus architectures. A typical switching fabric uses multiple stages of switches to route transactions between a source and a target. These dynamic paths are also valuable to high-availability designs, allowing you to route data around inoperable subsystems. Most of the major board standards now provide for switched fabrics, although they do not call out a specific fabric technology for data transport. Instead, a series of subsidiary specifications defines backplane details for the various fabrics, such as Ethernet, InfiniBand, StarFabric, PCI Express, and RapidIO. Although this approach satisfies differing views within the industry, it can also create interoperability issues within the same standard.

The VITA (VMEbus International Trade Association) 41 VXS (VITA switched serial extensions) add some of the high-availability benefits of fabric technology to the popular VMEbus (Versa-module eurocard bus). The VXS specification defines a payload card, a switch card, and a new high-bandwidth-backplane connector and retains the standard parallel-VMEbus connectors. Each new fabric port consists of two sets of four ganged serial-bit channels—one set for input data and the other set for output data supporting data rates of 10 Gbps for each serial channel. Switch cards contain the fabric switching necessary to route serial data between payload cards and around failures. To remain fabric-agnostic, VITA 41 subspecifications define switch and payload-card definitions for InfiniBand, serial RapidIO, GbE (gigabit Ethernet), and PCI Express.

Targeting the unique requirements of telecom equipment, the PICMG (PCI Industrial Computer Manufacturers Group) released the ATCA specification to provide an alternative to open architectures such as VME and CompactPCI. With emphasis on high-availability features, ATCA uses the high-speed serial-data links and switch-fabric technology. The extra-large board area supports the complex telecom circuitry and provides input power and cooling for as much as 200W per slot. The ATCA specification features hot-swap capability for all boards and active modules, allowing systems minimum downtimes. A shelf-management element, which the specification based on IPMI, monitors the health, power, cooling, and even keying of plug-in modules to ensure that subsystems are operating efficiently. Modules get power from redundant −48V-dc power feeds and data from redundant control and data planes to prevent a single failure from bringing down an entire chassis.

Taking advantage of the hot-swap and shelf-management features of ATCA and extending the performance envelope, Adlink Technology recently announced the aTCA-6900 CPU blade featuring two quad-core Intel Xeon processors and two AdvancedMC (mezzanine-card) bays for design flexibility (**Figure 1**). The aTCA-6900 CPU blade supports as many as eight CPU cores plus a fabric architecture that includes dual 10-Gbit Ethernet, dual PCI Express, and dual Fibre Channel interfaces. Onboard storage includes 4-Gbyte USB flash and a variety of hard-disk-mounting options. Front-panel I/O includes

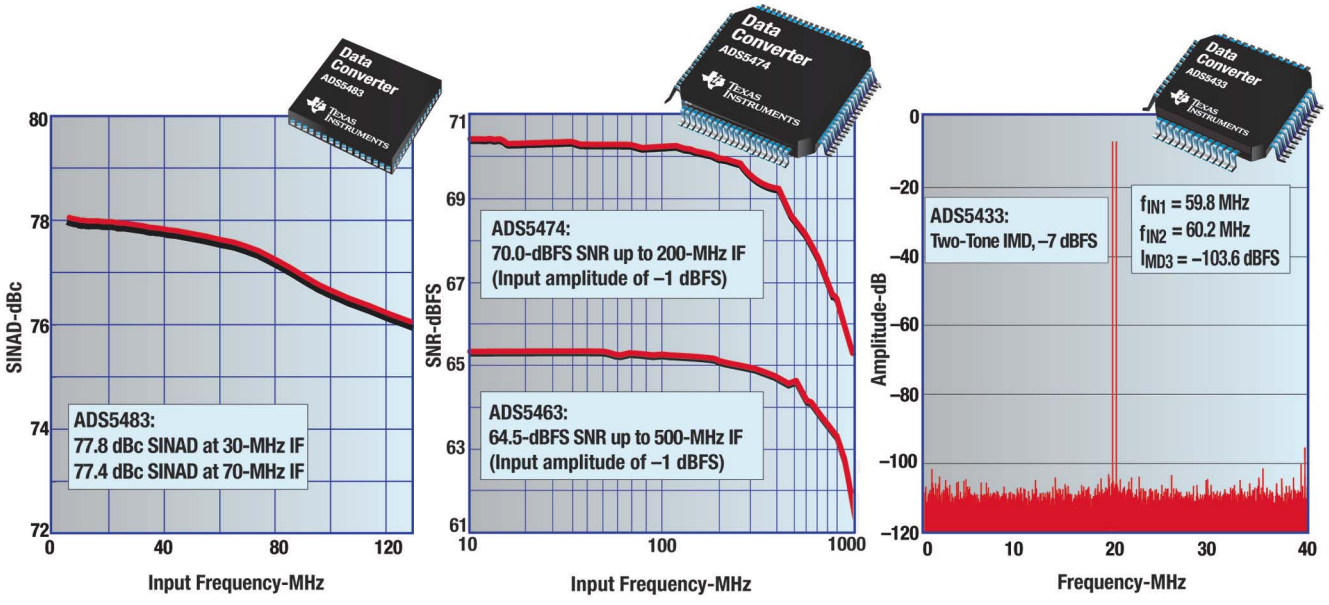
MORE AT EDN.COM

- For more on designing for reliability, go to www.edn.com/article/CA6535342.
- For more on hot-swapping and high availability, go to www.edn.com/article/CA46756.
- Go to www.edn.com/080515df and click on Feedback Loop to post a comment on this article.

Ultimate Performance ADCs

High Speed and Resolution with Buffered Inputs

High-Performance Analog>>Your Way™



TI's portfolio of small-form factor, high impedance input, bipolar junction transistor ADCs deliver the highest speed, resolution, dynamic performance and widest operational envelope in the industry. Whether you're designing for wideband communications, advanced avionics or test & measurement, TI provides your design with the performance characteristics required to win in the marketplace. **That's High-Performance Analog>> Your Way™.**

Device	Description
ADS5483	**16-bit, 135-MSPS ADC** with high SNR, SFDR and SINAD up to 130-MHz input frequency, with 77.8 SINAD at 30 MHz and 77.4 SINAD at 70 MHz IF. Available in a 9 mm x 9 mm QFN package. Pin-compatible with ADS5482 and ADS5481.
ADS5474	**14-bit, 400-MSPS ADC** provides typical SNR above 70 dBFS and SFDR greater than 80 dBc for input frequencies from DC to 200 MHz. Available in a 14 mm x 14 mm HTQFP package. Pin-compatible with ADS5463, ADS5444 and ADS5440.
ADS5433	**14-bit, 80-MSPS ADC** optimized for spurious-free dynamic range with 91-dBc SFDR guaranteed for a 30-MHz input across the I-temp range (–40°C to 85°C). Available in a 12 mm x 12 mm QFP package. Pin-compatible with ADS5423, ADS5424 and AD6644/45.
ADS5463	**12-bit, 500-MSPS ADC** offers high SNR and linearity with 10 ENOB through second Nyquist. Ideal for wide bandwidth, under sampling applications. Available in a 14 mm x 14 mm HTQFP package. Pin-compatible with ADS5474, ADS5444 and ADS5440.

www.ti.com/ads5474 1.800.477.8924 ext. 14453

Get samples and evaluation modules

Texas Instruments

video, three USB 2.0 ports, two RJ-45 Ethernet ports, and an RJ-45 serial port. Prices for the aTCA-6900 start at less than $5000.

SURE-FIRE STREAMS

As the number of networked embedded devices grows, the need for a dedicated and reliable data source becomes a major consideration in any new-product development. If you deploy multiple devices and each requests a different but simultaneous data stream, the data-server-processing requirements become critical. Many embedded-system applications, such as file sharing, security surveillance, and entertainment, require an independent and always-on data stream from a dedicated server. To meet the availability expectations of these data-centric projects, designers are turning to high-density computer arrays with hundreds of CPUs per rack and multiple CPUs per board. A system with multiple computer boards is typically called a blade server and features system management, load balancing, hot-swap capability, and shared peripherals to provide the high-reliability data for Web access and data services. Individual blade computers generally have no local peripherals, and you manage them remotely. Cluster-type servers run management software to balance the computing load, report failures, provide blade-configuration information, and oversee hot-swap transactions. Blade servers are basically high-availability systems that require special software to manage the system for maximum uptime. A separate management network increases server security by keeping critical operating-system information and updates from passing over public networks or the Internet.

Several open-source and commercial software organizations are dedicated to improving the reliability of operating systems and embedded firmware. For example, the High Availability Linux Project hosts an open-source-development effort to provide a clustering architecture for the Linux operating system to promote reliability, availability, and serviceability. Heartbeat, the most well-known component of the project, sends periodic packets across the network to the other instances of Heartbeat to verify performance. When the system no longer receives packets, it assumes a node failure and automatically reroutes services to an alternative node, according to a user-supplied formula.

Similarly, the Service Availability Forum comprises communications and computing companies working to develop high-availability and management-software-interface specifications. These specifications target the developers of telecommunications systems and services built with COTS building blocks, such as CompactPCI and ATCA. The objective is to allow for greater hardware and software reuse plus shorter product-development cycles. The hardware-platform-interface specification defines the interface between the COTS hardware and the high-availability management middleware (**Figure 2**). Applications can then independently discover, monitor, and manage the hardware without proprietary software interfaces.

Thanks to the latest generation of board standards plus a dedicated community of software developers, designers now have the tools to configure high-availability embedded systems using off-the-shelf products. Despite the trend toward multifunction and complex embedded products, designers can combine components from a variety of suppliers to match their performance requirements and still attain or even exceed the elusive "five-nines" (99.999%) availability target. EDN

FOR MORE INFORMATION

Adlink Technology
www.adlinktech.com

Dell
www.dell.com

Hewlett-Packard
www.hp.com

High Availability Linux Project
www.linux-ha.org

Intel
www.intel.com

NEC Electronics
www.necel.com

PICMG (PCI Industrial Computer Manufacturers Group)
www.picmg.com

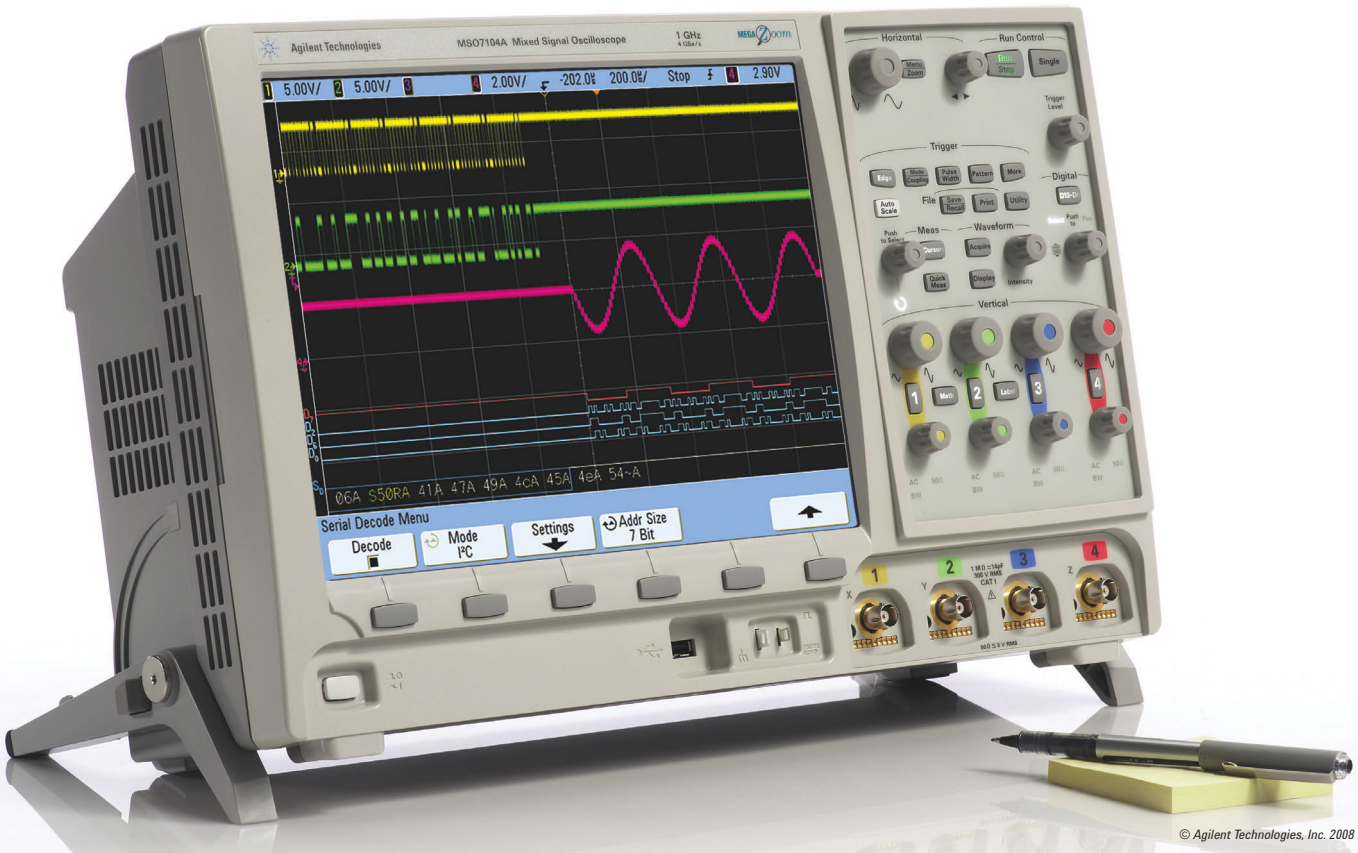
Service Availability Forum
www.saforum.org

VITA (VMEbus International Trade Association)
www.vita.com

You can reach Technical Editor Warren Webb at 1-858-513-3713 and wwebb@edn.com.

Biggest Screen. Best signal visibility.

Introducing Agilent's newest oscilloscope.



Agilent InfiniiVision 7000 Series oscilloscopes	
Bandwidth	350 MHz, 500 MHz, 1 GHz
Channels	2 or 4 analog +16 digital on MSOs
Waveform update rate	Up to 100,000 waveforms per second
Connectivity	USB, LAN, XGA-out
Display	12.1" XGA LCD
Footprint	6.5" deep, 13 lbs.
Applications	I^2C, SPI, CAN/LIN/FlexRay, RS-232/UART, Xilinx and Altera FPGA, Segmented Memory, Vector Signal Analysis, Offline PC-based analysis of acquired data, Power

5 new digital scope models and 5 new mixed-signal scope models

u.s. 1-800-829-4444
canada 1-877-894-4414

www.agilent.com/find/7000appnote

More than a decade ago Agilent introduced the industry's first mixed signal oscilloscope. Now you can experience 3rd generation MSO technology and the industry's fastest DSO update rates with the new InfiniiVision 7000 Series.

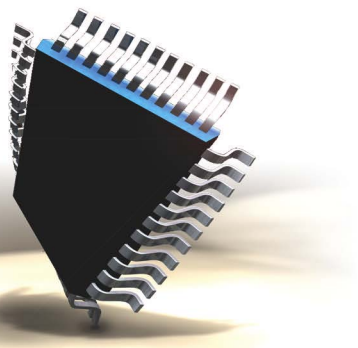
1. **Industry's biggest (12.1") screen** so you see analog, digital and serial signals better – in one instrument.
2. **Fastest uncompromised update rate** shows you critical signal detail and infrequent events that other scopes miss.
3. **Industry's only hardware accelerated serial decode** gives you faster insight.

See an online demo and get a free app note at www.agilent.com/find/7000appnote

Agilent Technologies

EVOLVING APPROACHES TO SOFTWARE DEVELOPMENT ARE PROVIDING DESIGNERS WITH MORE FLEXIBILITY IN CHOOSING AND MOVING AMONG PROCESSING CHOICES.

FLEXIBLE SILICON



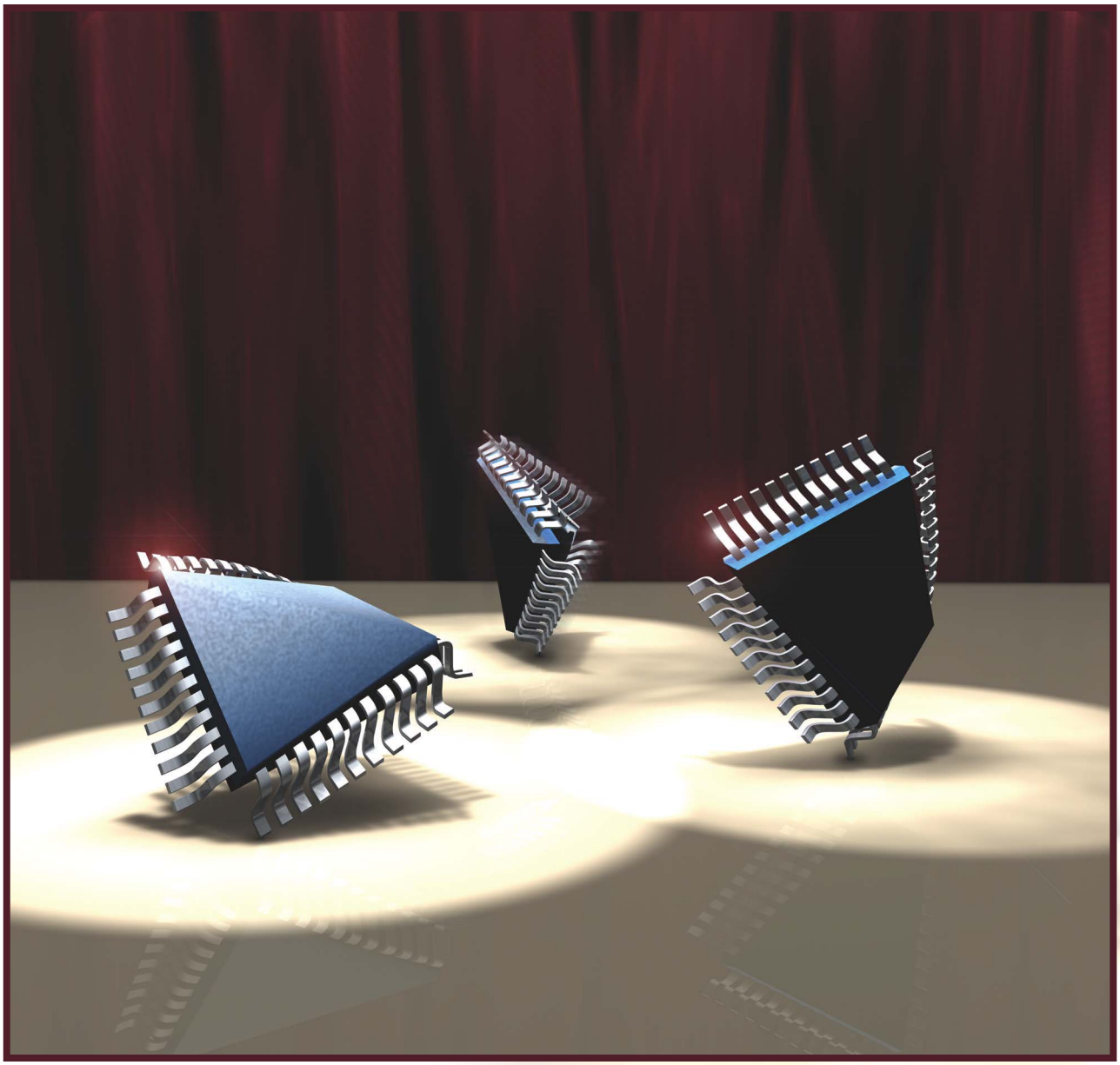
BY ROBERT CRAVOTTA • TECHNICAL EDITOR

Semiconductor companies are integrating more software content with their processor offerings, marking a stark contrast with days past, when companies left software development and tools as an exercise for designers to perform on their own. The earliest efforts to integrate software with a hardware offering were development tools, such as assemblers and compilers, to ease programming a target processor. The software that semiconductor companies and their development-tool partners provide to support embedded-software development has continued to expand over the past few decades. But the focus of these efforts has been on easing and speeding the use and development with a target processor or family of similar processors (see **sidebar** "Software productivity"). An emerging trend in how semiconductor companies and their partners are integrating software and hardware is going beyond just making development faster and easier; it is making hardware more flexible and enabling designers to explore more options before binding and optimizing their design to a processing target.

A challenge for software development for the embedded-processor market is how to productively work with the myriad processor architectures that are available to designers (**references 1** and **2**). One reason there are so many processing options is that it is a critical consideration for embedded designs to find a good balance of delivered functions, features, and power consumption that you can implement with minimum resources to enable lower costs. There are dozens of semiconductor companies that provide processors to embedded-system designers, and a handful of distinct processing approaches focus on how best to solve problems (**Reference 3**). Examples include microprocessors, microcontrollers, DSPs (digital-signal processors), programmable-logic fabrics, and DSCs (digital-signal controllers). Each of these processing options choose architectural trade-offs that emphasize optimized capabilities for the type of tasks they best address, often at the expense of other architectural constraints that play a negligible role in quickly and efficiently performing those tasks.

Further increasing the complexity of embedded-software development is the use of multiple processing options within a single system, such as a DSP, a microprocessor, and accelerated logic. Although most users focus their attention on the CPU inside a desktop computer, a handful of embedded processors inside that computer handles the peripherals, such as the disk drive, the network connection, and the video display. Automobiles rely on dozens of processors. Even consumer appliances, such as washing machines, microwave ovens, and refrigerators, can use several microcontrollers to control motors and the user interface and to monitor the overall system. These multiple processing units provide just enough performance at lower power consumption and lower cost.

The range of code-incompatible specialized processing options available forces software-development teams to bind



their design to target processor architectures as one of the first actions they must make. This decision significantly impacts the project's overall cost, design difficulty, and risk at a time when the team has the least information about what resources the project will ultimately require.

FLEXIBLE HARDWARE

A growing and key realization by the semiconductor companies is that the supplied software, runtime blocks, and development tools are no longer just adjuncts to make it easier to market and sell their silicon but are essential components of their entire system offering. In fact, the total resources a semiconductor company will invest in software to go with its silicon offerings represent a large and significant portion of the development budget. The days of processor companies saying they are not in the software business are at an end. The focus of semiconductor companies is moving to systems houses that have partitioned some of the system as hardware and software; they leave the remaining software capacity for designers to add their differentiation.

Semiconductor companies are creating and maintaining more software with their silicon products because software is a cheaper, safer, and more flexible way for these companies to continue the integration story of the past decade. Processor devices have been integrating more of the system into a single chip, including peripherals, memory, and memory controllers. However, it is not always practical to integrate everything as hardware. For example, the CRC (cyclic redundancy check) is an expensive function to perform in software but relatively simple to implement in hardware—yet only a handful of processor offerings, such as from Microchip, actually include an integrated CRC register. Including the CRC register in every processor does not make sense because many applications do not need it, but cases in which the primary application of the processor would use it enough justify its inclusion in the chip.

An emerging consequence of processor vendors' changing perspective toward integrated software is that it holds tremendous benefit for the vendors and designers if they can support flexibility among their processor offerings. Most processor companies offer multiple processor architectures so that they can better target more than a single application. Providing useful integrated software for all of those products is a difficult proposition, especially if there is no way to support software flexibility among all of those architectures. In fact, although some companies support flexibility within a subset of their processor offerings, providing a consolidated, comprehensive, integrated software suite across all of the company's architectures is still a goal for the future. This approach differs from a single integrated software-development environment that can support development across a semiconductor vendor's entire line of processors.

AT A GLANCE

- The industry is grappling with how to preserve or improve software productivity despite a growing number of architectures.
- Integrated, or bundled, software is an increasingly important way for processor vendors to differentiate their devices.
- A number of common and application-specific approaches are emerging and evolving to enable designers to explore and move among more processing options than ever before.

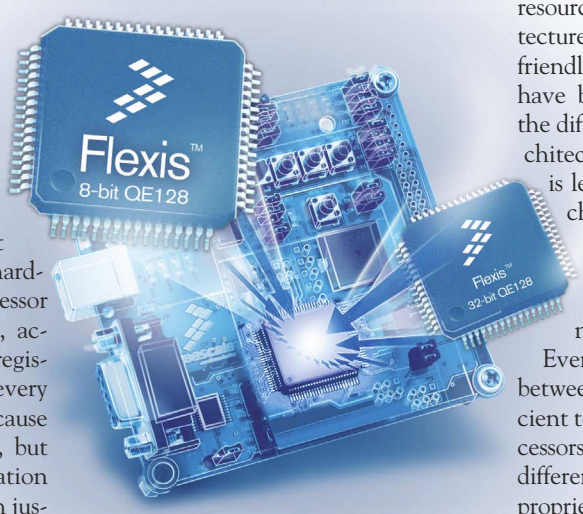


Figure 1 Freescale's Flexis processor platform affords designers the flexibility to explore and move between smaller 8-bit and larger 32-bit architectures and preserve their efforts in designing the board and software.

Adding to the complexity is the trend in variations of processor architectures. According to Clyde Stubbs, chief executive officer of Hi-Tech Software, the number of processor architectures has actually been proliferating, contrary to industry expectations. In a sense, this proliferation of instruction-set architectures is a testament to the success of modern compilers, because they have done an acceptable job of abstracting a target processor's instruction set. Although some of the variations are from architectural features, such as specialized execution engines, memory architectures tolerant of memory-access latencies are large drivers for architectural differences. This architectural variability is not capricious; it is the result of real differentiation, as architectural design teams make trade-offs for processors that target specific application categories.

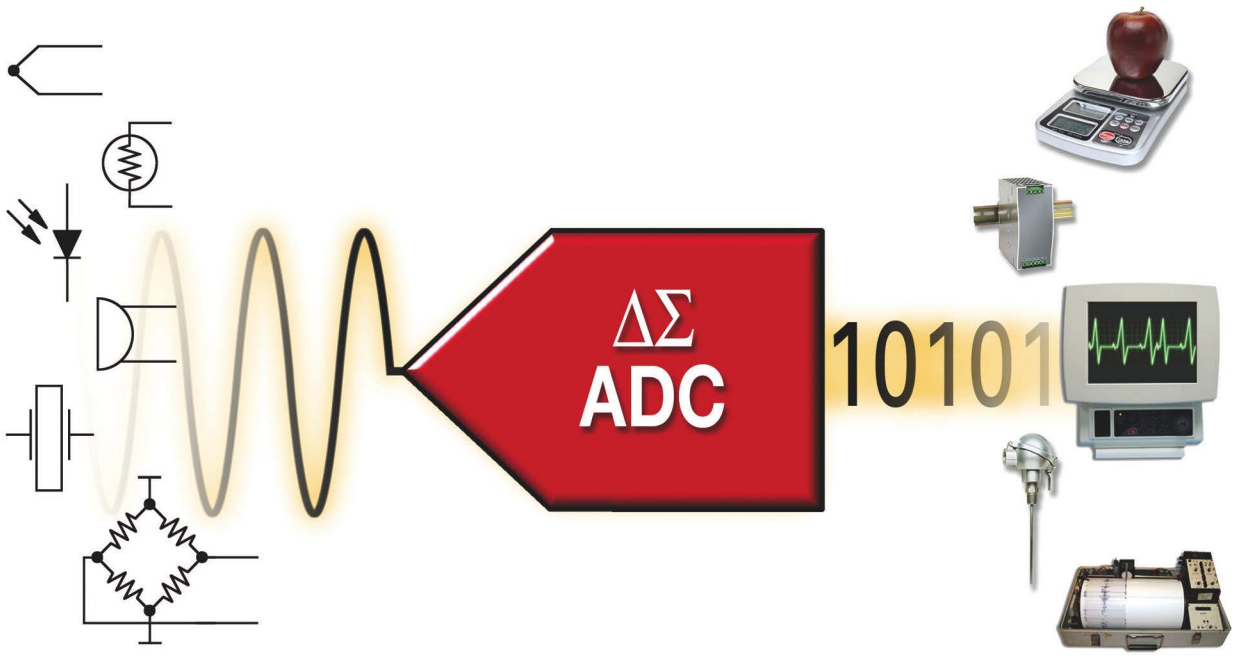
This type of variability impairs the usability of third-party IP (intellectual-property) blocks and portability of efficient code, especially for real-time-sensitive code. Programming languages, such as C and C++, do not include constructions to accommodate these architecturally important differences. As a result, compilers must use proprietary-language extensions if they are to be able to effectively employ these differentiating resources. So, although processor architectures have become more compiler-friendly at the instruction level, they have become less compiler-friendly on the differentiating features of modern architectures. A processor's instruction set is less a differentiator; its memory architecture and how it can perform relevant operations in parallel or with less power are larger factors. Unfortunately, these tasks are not compilers' strong suits.

Even using the same instruction set between processor offerings is insufficient to allow easy flexibility among processors. One of the ways ARM licensees differentiate their ARM7 devices is with proprietary interrupt, bus, peripheral, and memory-access structures. Although this approach enables the processor to handle a type of workload, it complicates porting code between two devices using the same CPU. ARM's Coretex architectures are partial moves to help with these types of software-porting challeng-

Delta-Sigma ADCs

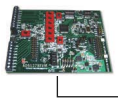
High Performance, Broad Portfolio—Enable Your Design

High-Performance Analog>>Your Way™



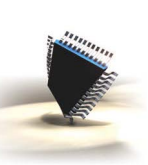
Low noise. Wide bandwidth. High speed. When your design needs best-in-class delta-sigma ADC performance, look to TI for high-performance devices to meet your design challenges.

Device	Description
ADS1110	Tiny, low power, 16-bit ΔΣ ADC with onboard reference and PGA (G=1, 2, 4, 8) in SOT: 2.048V ±0.05% accuracy, 5ppm/°C drift
ADS1226	Low-cost, easy-to-use 24-bit ΔΣ ADC: dedicated START pin, 100SPS data rate, 4μV_{RMS} low noise
ADS1232	Ideal for weigh scales: 24-bit ΔΣ ADC, up to 23.5 effective bits, onboard PGA (G = 1, 2, 64, 128), 10SPS or 80SPS data rates
ADS1256	Best-in-class 23-bit, noise-free ΔΣ ADC: 8 channels, 30kSPS and programmable digital filter (averaging)
ADS1258	Fastest channel cycling, 24-bit, 125kSPS ΔΣ ADC: Measure all 16 channels in <675μs
ADS1278	Widest bandwidth, simultaneous sampling: 24-bit, 8-channel ΔΣ ADC, 128kSPS, 106dB SNR, ±0.0003% INL
ADS1281	Ultra-low distortion 24-bit ΔΣ ADC: 130dB SNR and –122dB THD while consuming only 12mW of power, ±0.00006% INL
ADS1610	Fastest 16-bit ΔΣ ADC: 10MSPS, 86dB SNR, 5MHz wide and flat bandwidth
DDC232	Highly integrated, current-input 20-bit ΔΣ ADC for measuring photodiodes, X-ray security and CT scanners: 32 channels



www.ti.com/deltasigma 1.800.477.8924 ext. 1434
Get Datasheets, Samples and Evaluation Modules

Texas Instruments



es, such as by specifying a consistent approach for handling interrupts.

TOUCH POINTS

Enabling designers the flexibility to explore more processor architectures and delay binding to a given device requires action by the semiconductor companies and their software-tool partners. Many companies use common peripheral blocks among their processor offerings and support a consistent interface to each type of peripheral. To aid designers with configuring and using peripherals, many companies now offer device managers, configuration wizards, processor experts, or visual-device-initializer tools that allow designers to work at a higher level of abstraction and avoid the learning curve of how to explicitly place a peripheral into a specific state. This approach enables designers more flexibility to move among devices that these tools support; it does not, however, eliminate the need for de-

SOFTWARE PRODUCTIVITY

Processor architectures and software-development tools have changed significantly since the vendors introduced the first assemblers to ease and speed up the programming of those early processors for developers. Assemblers were basically a one-to-one mapping of the underlying processor architecture into a set of mnemonics that made translating logic statements into machine code easier and more reliable. A goal for the high-order-language compilers that followed was to abstract the low-level complexity of programming so that programmers could focus on the intent of the logic rather than the low-level coding implementation.

A challenge for early compilers was that vendors often designed processor architectures for the benefit of the architecture team rather than the software team, which resulted in compilers generating fairly poor code compared with a hand-optimized-assembly approach. Part of the reason for this poor performance was that early processor architectures relied on specialized resource structures, such as special-function registers and address banks. To efficiently use these specialized resources, the designer must make and keep track of a set of assumptions to avoid resource conflicts that would otherwise result in incorrect system behavior. Programming languages do not even acknowledge these special resources, and there is no standard way for a compiler to know the assumptions applied to each special resource, so compilers must make the most conservative set of assumptions to make safer but less efficient code. Many modern compilers implement proprietary directives that allow developers to direct the compiler to use a looser set of assumptions to generate more efficient code.

The next software-productivity gain did not manifest itself as a purely software play like the assembler and compiler but rather came about because processor-architecture designers started to work with the software-tool developers to make architectures that were more compiler-friendly. By making instructions and resources orthogonal, compilers could use a better and more reasonable set of assumptions when generating code, and compiler technology could mature enough that it would not require hand-optimization.

Many modern compilers do an excellent job of resequencing instructions to work well with the processor's instruction-fetch and -execute mechanism and minimize processor stalls. However, the problem of modern compilers continues to be how to best allocate and use the processor's special resources, especially those that compensate for the latency inherent in other parts of the system, such as bus and memory accesses. The resources include such things as specialized bus, memory, and DMA structures that give the processor an advantage over other processors for some set of tasks. Even today, a designer usually must explicitly allocate and declare how to best use the resources. Development tools, unlike compilers, do not usually incorporate features to achieve this goal, but the information is often available as application notes. This situation presents an area of opportunity for compiler and software-development tools, but no obvious way to accomplish this task yet exists.

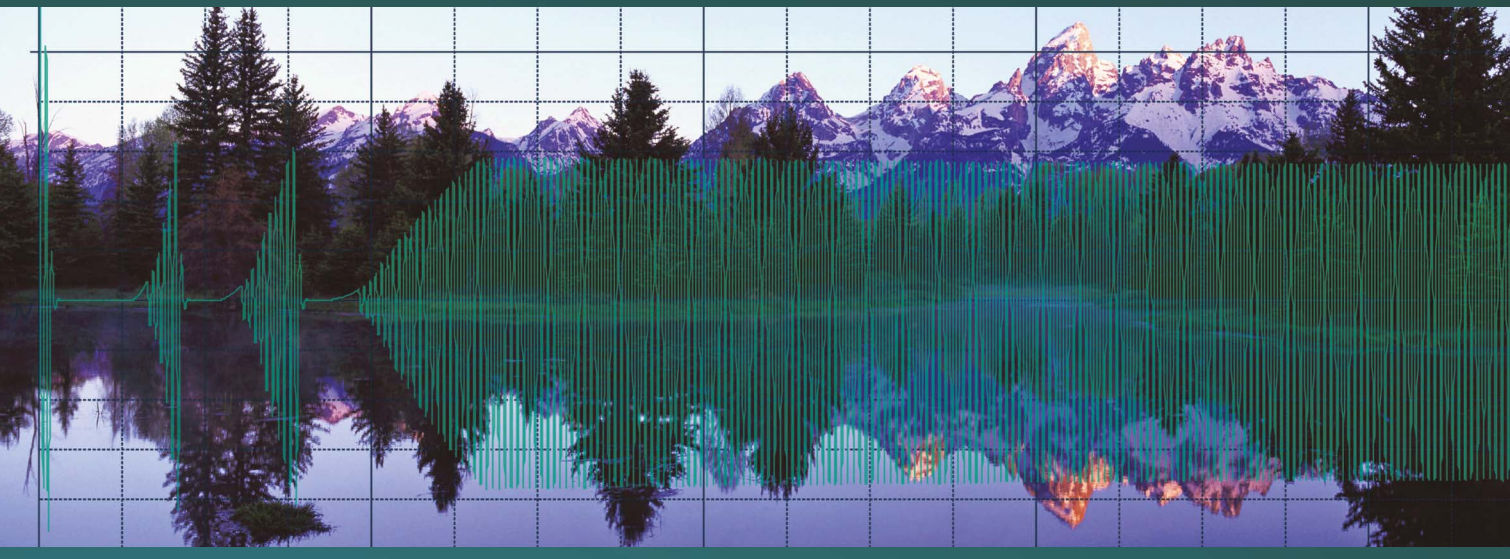
The next level of software-productivity gain came from integrated development environments that presented and provided access to a variety of tools, including program editors, profilers, debuggers, and project managers, in a single environment. These environments have evolved so that they can present a consistent way to develop software across a variety of processor targets; they allow designers to avoid the full learning curve of using a different tool set and processor with each project. Some development environments, such as for Texas Instruments' DaVinci and Freescale's Flexis, are evolving to enable designers to change the target processors later in the design cycle.

The arsenal of software-development tools continues to grow and improve software productivity, but changes in the hardware accompany each improvement. Privileged hardware resources allow operating systems to be more effective. Dedicated on-chip hardware-debugging resources are essential to enabling visibility into what is going on inside increasingly complex processor devices. Semiconductor companies not only support peripheral-configuration wizards to help designers, but also are adopting a common set of peripheral blocks, or interface wrappers, within their own product lines to reduce complexity that software-development tools and developers must contend with. As the number of transistors available to implement a processor continues to grow, the number of transistors that the processor will dedicate to improve software productivity will also continue to grow.

Cadence PSpice Technology

Helping you see the forest for the trees

Simulation



PCB

SI

Custom IC

Analog

Digital

Libraries

Mechanical

PLM

Training

Advanced simulation for analog and mixed-signal environments
Constrained by increased design complexity and shorter design cycles, PCB design teams need fast and reliable simulation to achieve design completion. Cadence® full-featured analog simulator with support for digital elements helps solve virtually any design challenge—from high-frequency systems to low-power IC designs. The powerful simulation engine integrates easily with Cadence PCB schematic entry solutions, improving time to market and keeping operating costs in check. An interactive, easy-to-use graphical user interface provides complete control over the design process.

Advanced analysis for maximum circuit performance
Only Cadence PSpice® simulation offers the technology needed by professional engineers to solve their complex design problems. The advanced analyses allows designers to automatically maximize the performance of circuits. With features like sensitivity analysis, optimization, Smoke (stress audit), and Monte Carlo (yield analysis), engineers don't just determine if their designs work, they make them work better.

Designers can now perform system-level simulations that include realistic electrical models of actual components. The integration of PSpice technology and MATLAB® Simulink® (SLPS) brings two industry-leading simulation tools into a powerful co-simulation environment.

Boost your productivity with Cadence PSpice simulation today!
Experience the new features of PSpice 16.0 by visiting EMA, a Cadence Channel Partner, online at www.ema-eda.com/PSpice or call us at 800.813.7288

cadence™
CHANNEL PARTNER

EMA Design Automation™
ema-eda.com

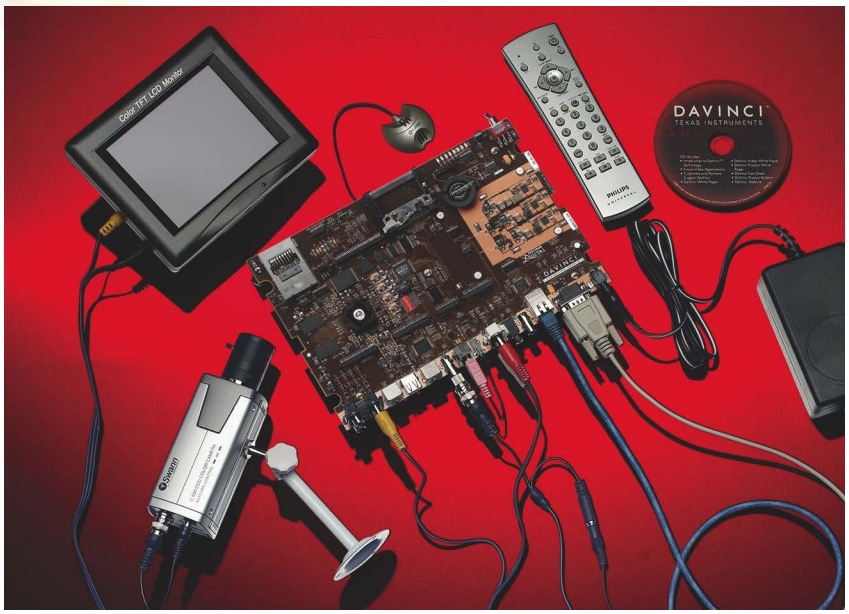


Figure 2 Texas Instruments' DaVinci platform targets applications with video capabilities, but the software-development model enables developers to more easily shift their software to different silicon offerings with heterogeneous processing engines.

signers to understand the consequences between the processing performance and power consumption of specialized blocks, such as hardware accelerators or smart peripherals, versus generalized blocks.

Differentiating approaches to supporting flexibility in silicon choices include Microchip's common-code base, which allows designers to migrate between 16- and 32-bit PIC devices and offers common APIs (application-programming interfaces) to abstract architectural differences and present virtual peripherals. It also gives peripheral blocks a defined, consistent look, feel, and behavior and provides the ability to remap I/O pins with a peripheral pin-select capability.

MORE AT EDN.COM

- For related blog posts about embedded processing, go to www.edn.com/blog/1890000189.
- For a related article about processing options, go to www.edn.com/article/CA6298267.
- For a related article about abstracting complexity, go to www.edn.com/article/CA426084.
- Go to www.edn.com/080515cs and click on Feedback Loop to post a comment on this article.

Renesas announced the RX family of processors to unify the peripheral IP between legacy 16- and 32-bit processors from Mitsubishi and Hitachi as an extension of those architectures. The EXREAL (Excellent Reliability Efficiency Agility Link) Platform is a "mother," or superset, platform targeting the development of specialized processor platforms using common software-evaluation, -development, -optimization, and -validation techniques to enable more architectural exploration.

Freescale's Flexis platform attempts to provide more flexibility among price, performance, and power trade-offs by providing a software-development environment that spans 8- and 32-bit architectures and supports movement both up and down among those architectures (**Figure 1**). According to Jeff Bock, global product-marketing manager for consumer- and industrial-microcontroller operation at Freescale, 50% of Flexis designers know upfront which architecture they are going to target, 25% target both architectures, and 25% explore both architectures and delay their choice until they have application code and can compare the differences between both architectures.

Texas Instruments' DaVinci development approach, an evolutionary step beyond the earlier OMAP (Open Multi-

TOUCH POINTS ARE SIGNIFICANT CONCERNS TO PROCESSOR SUPPLIERS BECAUSE SOME DESIGNERS WANT TO WORK AT THE APPLICATION LAYER; OTHERS WANT TO TOUCH THE SYSTEM AT LOWER LEVELS.

media Applications Platform) approach, takes the most extreme stance on silicon implementation. DaVinci devices may include any combination of microprocessor, microcontroller, DSP, FPGA, or even hardware accelerators. A consequence of this approach is that, although designers may use multiple heterogeneous cores, the software-development model attempts to abstract the implementation through APIs so that, as new silicon offerings become available, designers can migrate more easily to better silicon targets without a major porting effort. Greg Mar, DSP-strategic-marketing manager at Texas Instruments, points out that, despite efforts to preserve a designer's software investment, the need to support different "touch points," or levels of interaction, even from the same customer, creates significant challenges.

Touch points are significant concerns to any embedded-processor supplier because, although some designers want to work at the application layer, which is ideal for APIs and preserving software investments, others want to touch the system at lower levels, such as at the hardware-abstraction layer all the way down to the silicon with assembly programming. This situation creates a major challenge because each developer wants to see different information as he develops his system.

You can reach
Technical Editor
Robert Cravotta
at 1-661-296-5096
and rcravotta@edn.com.

A key element of modern processor systems and their surrounding ecosystems is that they enable designers to perform more exploration than they ever could before. Many processors offer evaluation or demonstration boards. A key goal of modern low-cost evaluation kits is to enable designers to quickly explore a family of processors and determine whether it is a good candidate for their project. The attention to detail in modern evaluation kits focuses on getting the designer up and running in minutes by integrating the hardware with vertically targeted software. These systems also save designers time by immediately confirming that the system is indeed operating correctly when the designer first connects it to his workstation and helping to avoid opportunity-destroying troubleshooting in kits that do not work properly out of the box. They allow designers to explore more processing options and give semiconductor companies more access to the designers.

Getting a working implementation of a processor into a designer's hands also means suppliers can offer differentiating software to expand, optimize, and better target the platform to a designer's project by making common, optimized software libraries that support the range of processor options that the kit represents. It is increasingly in the interest of designers to use the integrated software, so that they can incorporate the lessons they learned into future versions from the processor provider. It is also in the processor vendor's interest to maintain this integrated software in more than an as-is condition, because it is an integral part of its system offering that happens to include hardware and software partitioning before the designer even considers the part. EDN

REFERENCES

1 Cravotta, Robert, "*EDN* Microprocessor/Microcontroller Directory," www.edn.com/microdirectory.
2 Cravotta, Robert, "*EDN* DSP Directory," www.edn.com/dspdirectory.
3 Cravotta, Robert, "Processing options," *EDN*, Jan 19, 2006, pg 42, www.edn.com/article/CA6298267.

FOR MORE INFORMATION

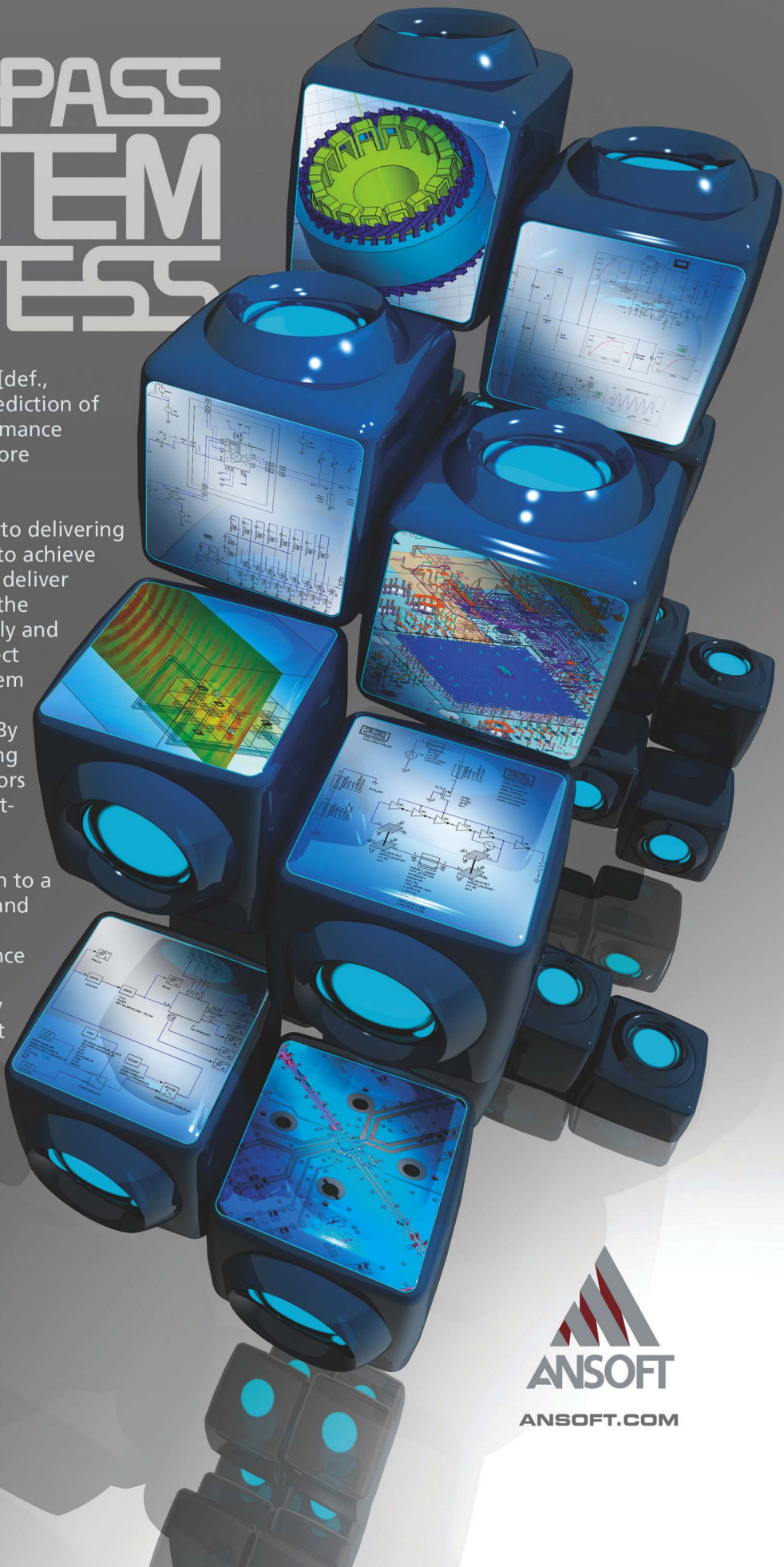
For more information about the companies mentioned in this article, go to www.edn.com/080515cs.

FIRST-PASS SYSTEM SUCCESS

First-Pass System Success, [def., Engineering] The accurate prediction of the behavior of a high-performance electronic product design before committing to hardware.

At Ansoft, we are committed to delivering design and analysis software to achieve First-Pass System Success. We deliver the power you need to solve the fundamental physics accurately and quickly and to use these correct models at the circuit and system levels to precisely predict the performance of your design. By leveraging our industry leading electromagnetic field simulators dynamically linked to our next-generation circuit and system tools, Ansoft has taken high-performance electronic design to a new level of accuracy, speed and precision. We deliver the capabilities you need to balance high-speed, low power, high density and process variability to get your product to market faster, at lower-cost and with higher performance.

Contact us, we will be happy to show you how to achieve **First-Pass System Success**.



ANSOFT

ANSOFT.COM

BY KEITH KLEPIN • CYPRESS SEMICONDUCTOR

Overcoming USB measurement-test-setup issues

DESIGNERS MUST MEET STRINGENT CONSTRAINTS TO COMPLY WITH THE USB-IF SPEC. CLEVER TECHNIQUES CAN HELP YOU DESIGN YOUR SYSTEM TO MEET THESE SPECS.

Measuring the signal quality of USB (Universal Serial Bus) interfaces requires that designers meet the stringent constraints of the USB-IF (USB Implementers Forum, www.usb.org) specification. Nothing is more frustrating, however, than attempting to hunt down signal-quality issues in your design when your test setup has introduced curve errors. By isolating setup-testing issues from design-testing issues, designers can ensure that they are making proper measurements of the signal quality of USB-data lines. This accomplishment will lead to uncovering rather than masking design problems.

The foundation of measuring USB-signal quality is a violation plot (**Figure 1**). This plot is the width of a single bit; three boundaries—upper limit, lower limit, and center eye—outline this plot of data, and these boundaries create the violation area and define the area that the signal must not pass through. If the signal enters the violation area, then the design has violated at least one of the USB-specification requirements. The violation area depends on the configuration of the DUT (device under test). For example, a "captive" cable has a different set of limits from a device using a standard B connector. The USB-IF specification contains the plots for each of these tests. Once you have selected the proper test limits for the configuration, you use a test packet to generate each bit over this template. If the signal is monotonic and does not pass through the violation areas, then the signal passes the signal-quality measurement. You must also consider the edge rate of the signal and ensure that the signal does not have too sharp a rise or fall.

DEVICE SETUP

The first step is to configure the limits of the test. You accomplish this task by selecting the proper location for measuring the signal, and this location depends on the DUT. If the device has a captive cable, you must measure the signal at the far end of the cable. If the device has a standard USB connector, then you measure full-speed signals at the far end of a 5m cable and high-speed signals at the near end of the cable. The far end is 5m from the device emitting the signal, and the near end is the connector of the device emitting the signal. Be sure to measure in the proper direction; that is, the data should be originating from the DUT rather than the host.

When working with high-speed signals, check the test switch on the test fixture. If the switch is in test mode—that is, the test LEDs are lit—then you can measure signals only from the DUT. If you are measuring full-speed signals, then signals are coming from both directions, and you must check the data to ensure that you are measuring it in the proper di-

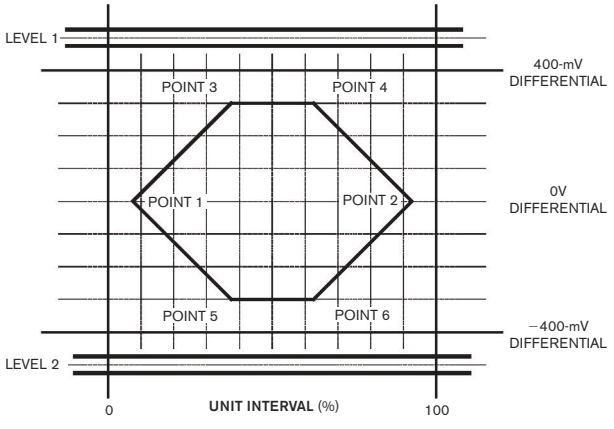


Figure 1 The foundation of measuring USB-signal quality is a violation plot that is the width of a single bit; three boundaries—upper limit, lower limit, and center eye—outline this plot of data.

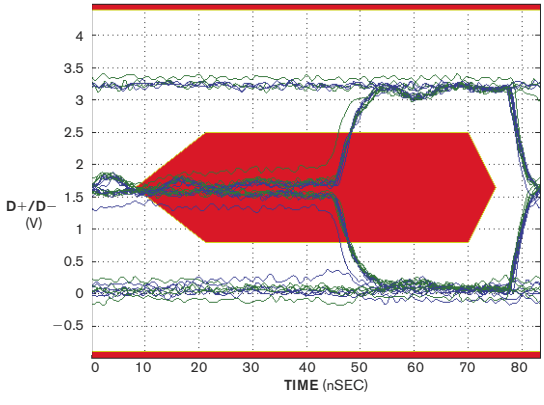


Figure 2 The null point has a width that directly relates to the length of cable over which you are making the measurement.

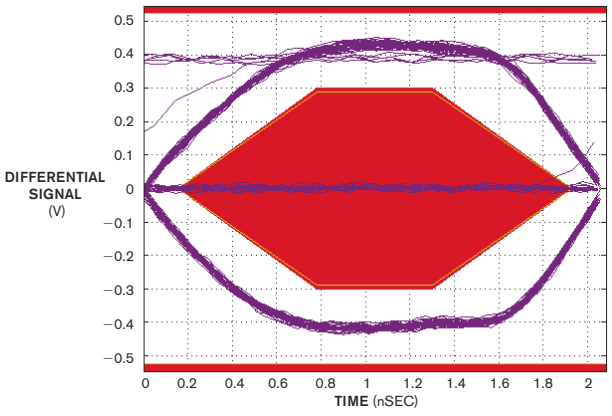


Figure 3 A typical setup problem you encounter when dealing with high-speed signals is accidentally connecting the differential probe backward.

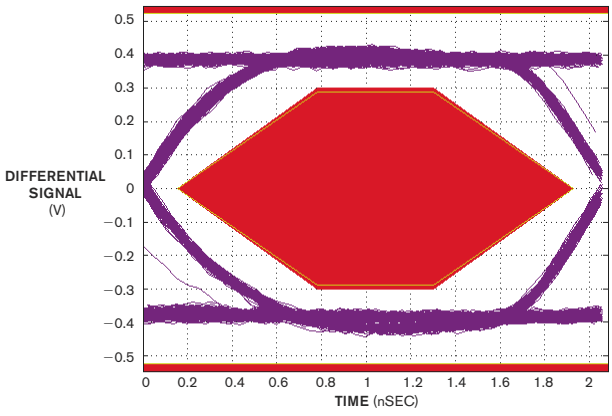


Figure 4 When you properly configure and connect the test setup, you should get a clean eye diagram.

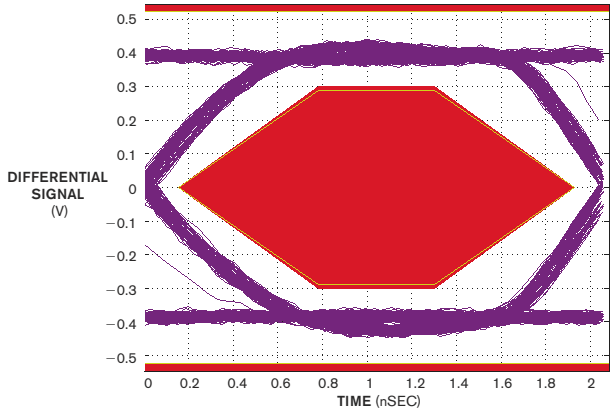


Figure 5 As little as 2-pF capacitance can cause the leading section to rise slower and round off the edge of the signal.

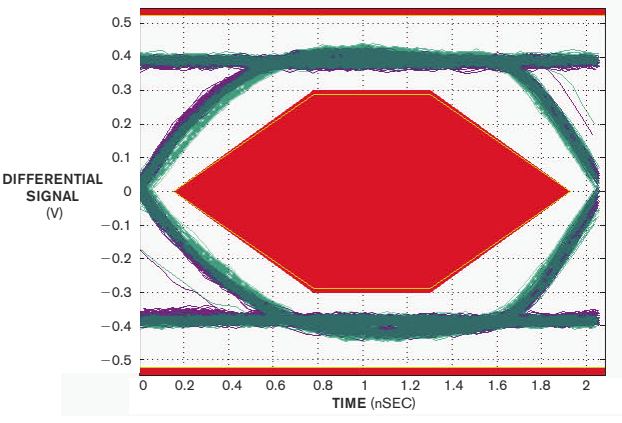


Figure 6 The effect of added capacitance on measurements shows both the desired eye diagram of Figure 4 (purple trace) and the eye diagram of Figure 5 when you add 2-pF capacitance to the test fixture (green-overlaid trace).

rection. To confirm the measurements, check to see whether the signal is traveling the length of the cable to the measurement point—that is, a far-end measurement.

The best method for accomplishing this goal is to look at the crossover points. If the signal is coming from the near end of the cable, it will travel past the measurement point, down the cable, and then back again, creating two images, with the second exhibiting a phase shift compared with the first. The results of summing these two images is a null point at the crossover. This null point has a width that directly relates to the length of cable over which you are making the measurement (**Figure 2**).

Another typical setup problem you encounter when dealing with high-speed signals is accidentally connecting the differential probe backward (**Figure 3**). The root cause of this error is that scripts that synchronize with data patterns make an assumption about the probe's polarity and expect signals to arrive in a given sequence. When you reverse the signal by connecting the probe 180° out of phase, you measure the D+/D− differential pair as a D−/D+ differential pair. This approach causes the algorithm to plot the leading edge of the signal, which creates lines through the center. Reversing the probe connection resolves this problem. When you properly configure and connect the test setup, you should get a clean eye diagram (**Figure 4**).

Unintended impedance adversely affects measurements. If you inadvertently add impedance, signal amplitude can decrease, edge rates can change, and overshoot can appear. Adding capacitance to traces, cabling, or the test fixture decreases the rise time of the leading edge. As little as 2-pF capacitance can cause the leading section to rise slower and round off the edge of the signal (**Figure 5**). **Figure 6** shows the effect of added capacitance on measurements; the **figure** shows both the desired eye diagram of **Figure 4** (purple trace) and the eye diagram of **Figure 5** when you add 2-pF capacitance to the test fixture (green overlaid trace). Most of the difference appears in the leading edge of the image; the rising and falling edges show a lowering of the signal edge rate by approximately half the width of the jitter. Rise time affects this signal, which also experiences a slight increase in jitter. Increasing added capacitance to 8 pF, for example, would begin to result in eye violations. Similarly, when you add inductance to the traces, the signal experiences overshoot and may round both the top and bottom of the eye.

Factors that can affect measurement range from trace impedance to the connector that the device uses. When using

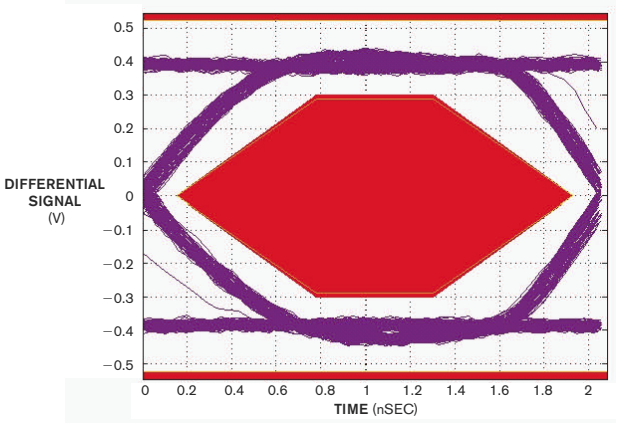


Figure 7 This adapter has a mini-B connector on one end and an A connector on the other.

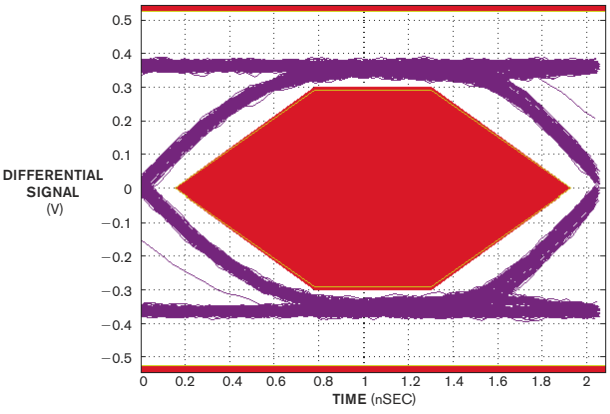


Figure 8 This measurement occurs when you use a standard 4-in. cable, which connects the B connector to an A connector along with an adapter to convert the mini-B receptacle to the B connector.

connectors other than certified USB connectors, you should verify that the impedance effects of these connectors meet the USB specification before testing the system.

CABLING ISSUES

When measuring USB-signal quality, another area of concern is in the connections that the device is making. For example, to connect a device with an A receptacle to a device with a mini-B connector requires an adapter and introduces extra connectors into the signal path. **Figure 7** shows the measurement across an adapter with a mini-B connector on one end and an A connector on the other. **Figure 8** shows the measurement when you use a standard 4-in. cable to connect a B connector to an A connector along with an adapter to convert the mini-B receptacle to the B connector.

These extra connectors decrease amplitude and lower the margin around the violation area. Minimizing the number of connections in the test setup helps you acquire a truer signal-

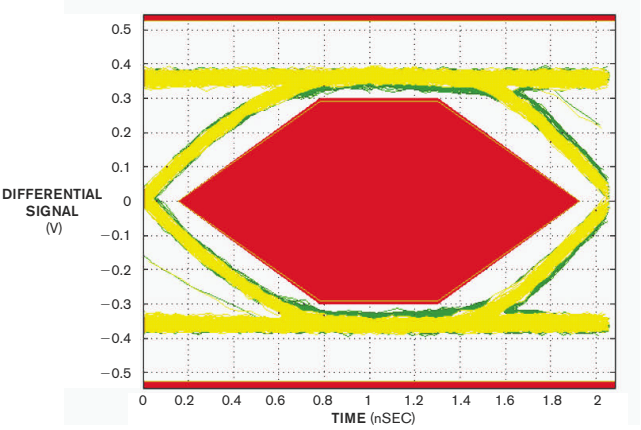


Figure 9 The impact of extra connectors is even more critical when the series impedance is already near the limits of the USB specification.

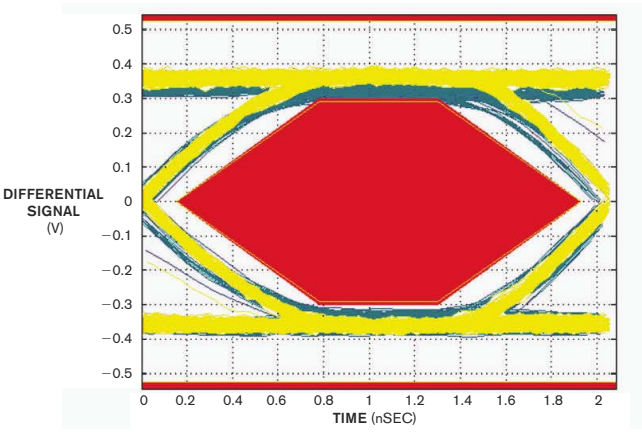


Figure 10 The bluish-green traces are uncalibrated traces, and the yellow traces show the effect of calibrating the probes. Failing to calibrate the probes affects both jitter and amplitude.

quality measurement. **Figure 9** shows the impact of an extra connector. (The yellow trace in **Figure 7** is the true reading, and the green trace in **Figure 8** shows multiple connections through the use of adapters). The impact of extra connectors is even more critical when the series impedance is already near the limits of the USB specification.

MORE AT EDN.COM

Go to www.edn.com/ms4280 and click on Feedback Loop to post a comment on this article.

CALIBRATION ISSUES

Another common setup problem is the failure to calibrate the scope probes. You should calibrate the probes if they are outside the calibration-temperature range or you have not calibrated them for months. **Figure 10** shows the impact of calibration on measurements: The bluish-green traces are uncalibrated traces, and the yellow traces show the effect of calibrating the probes. Failing to calibrate the probes affects both jitter and amplitude.

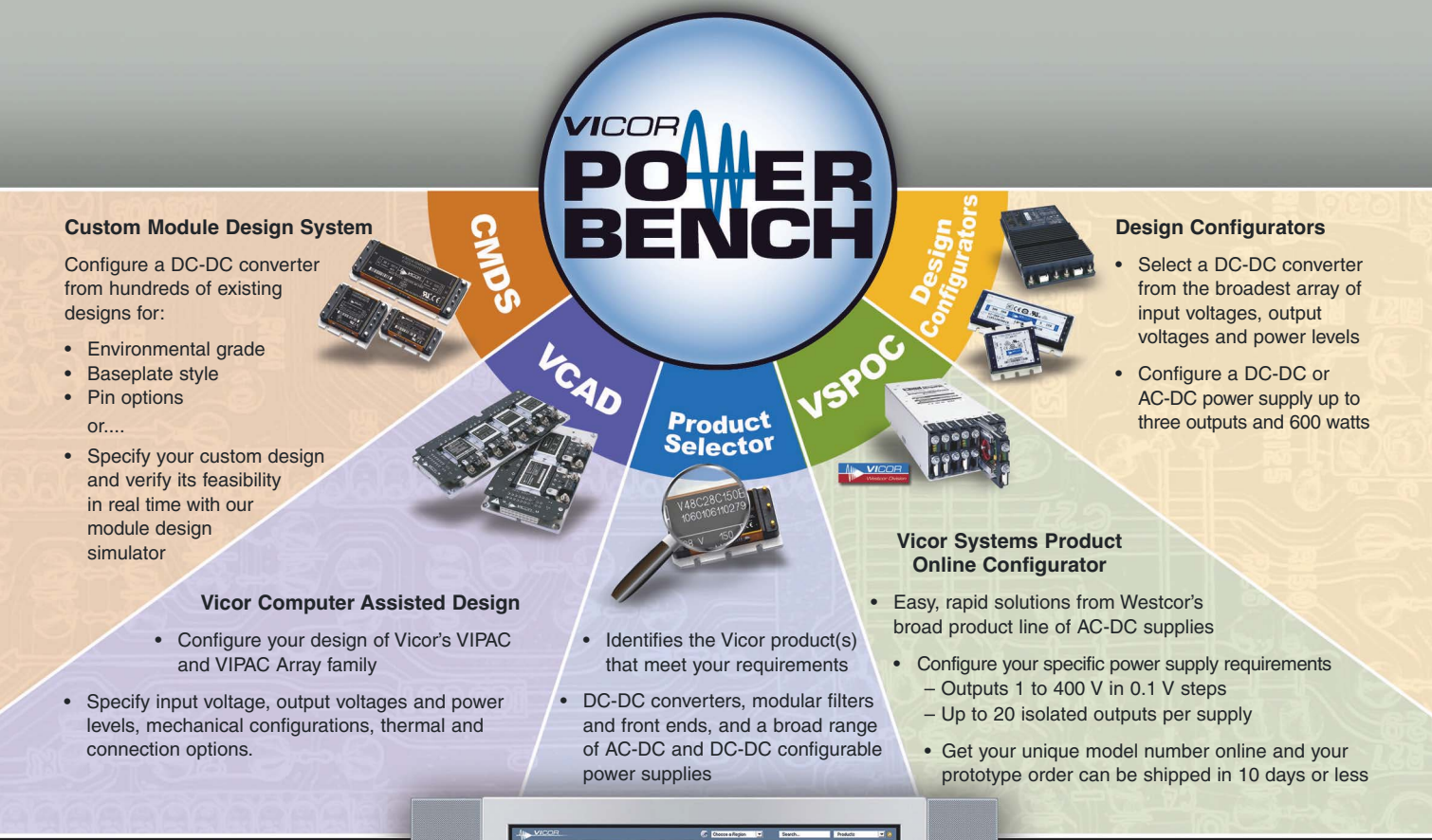
In summary, when measuring USB-signal quality, begin by following the procedures that the USB-IF Web site outlines. If problems appear, first confirm that your test setup and configuration are correct by ensuring that the intended measurement point is what you are measuring, that you are using the proper-length cable, that you have accounted for items such as adapters that you have placed in the signal path, and that you have recently calibrated your test tools. Each of these factors can induce errors that can cause compliant signals to appear to be in violation of the USB specification. Finally, consider that multiple issues may be in effect. Even though the impact of each factor may induce only a small error, several errors at the same time can cause failures. EDN

AUTHOR'S BIOGRAPHY

Keith Klepin is a senior staff application engineer at Cypress Semiconductor, where he has worked for seven years. Klepin is responsible for application development and USB-compliance testing. He received a master's degree in electrical engineering from San Diego State University. His leisure-time interests include photography, digitizing photos, and gardening.

You DESIGN It
We BUILD It

Use the Most Comprehensive Power Design Tools Available



Custom Module Design System

Configure a DC-DC converter from hundreds of existing designs for:

- Environmental grade
- Baseplate style
- Pin options

or....

- Specify your custom design and verify its feasibility in real time with our module design simulator

Design Configurators

- Select a DC-DC converter from the broadest array of input voltages, output voltages and power levels
- Configure a DC-DC or AC-DC power supply up to three outputs and 600 watts

Vicor Computer Assisted Design

- Configure your design of Vicor's VIPAC and VIPAC Array family
- Specify input voltage, output voltages and power levels, mechanical configurations, thermal and connection options.

- Identifies the Vicor product(s) that meet your requirements
- DC-DC converters, modular filters and front ends, and a broad range of AC-DC and DC-DC configurable power supplies

Vicor Systems Product Online Configurator

- Easy, rapid solutions from Westcor's broad product line of AC-DC supplies
- Configure your specific power supply requirements
  - Outputs 1 to 400 V in 0.1 V steps
  - Up to 20 isolated outputs per supply
- Get your unique model number online and your prototype order can be shipped in 10 days or less

PowerBench gives you the power to specify your own power design solution.

And verify it in real time. All on line.

It's fast, easy, and cost effective!

Visit the Vicor website at www.vicorpower.com/powerbench

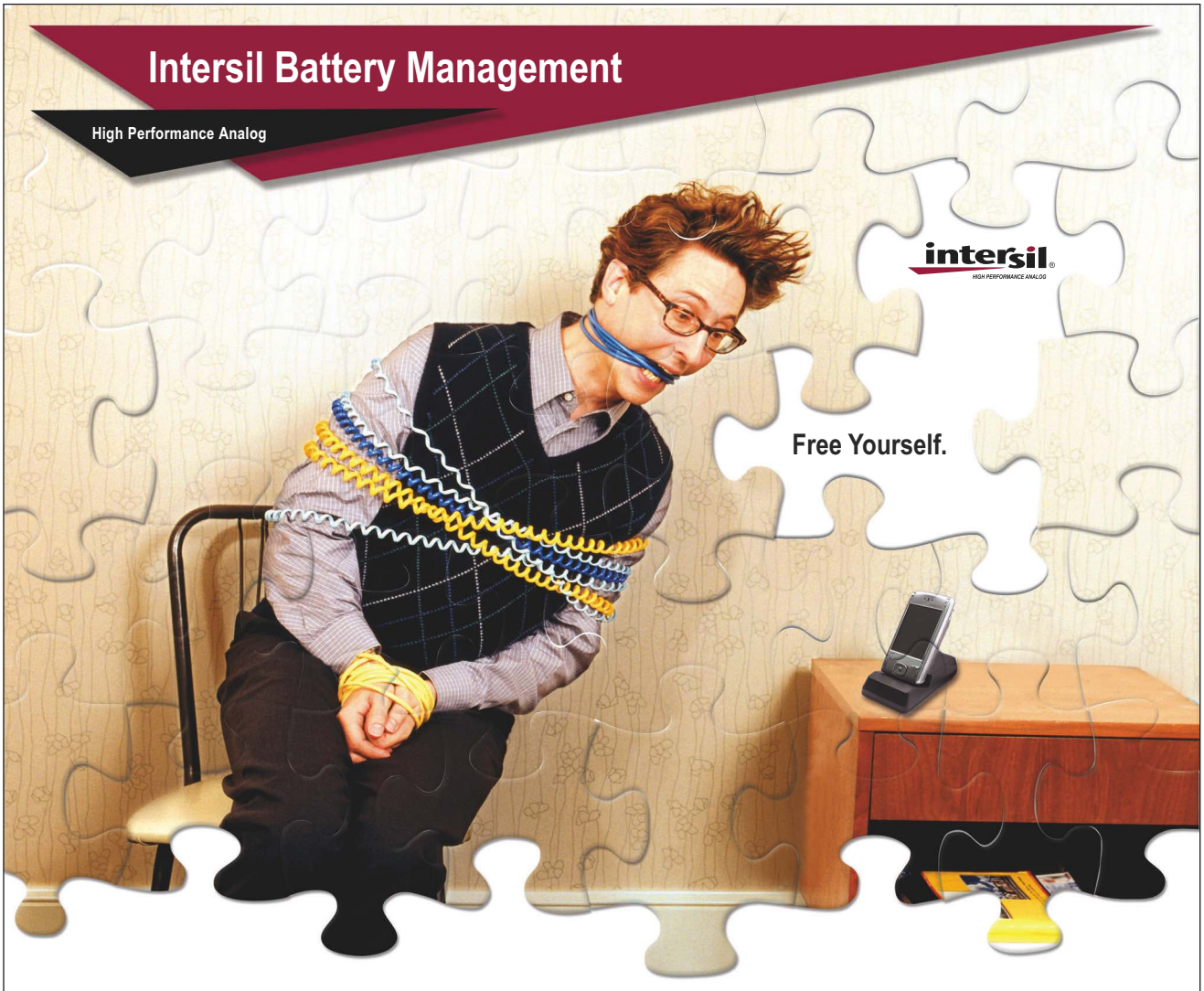
Call Vicor Technical Support at 800-927-9474

VICOR
power at your control

vicorpower.com/powerbench

Intersil Battery Management

High Performance Analog



Intersil's Li-Ion/Li-Polymer Battery Charger provides **28V protection for both cradle AND USB charging.**

ISL9214 Key Features:

- **28V protection for both cradle and USB input** allows users to utilize low-cost, large output tolerance adapters.
- **Charge current Thermaguard™** protects IC against over-temperature events.
- **Programmable charge current/end-of-charge current** allows designer to customize to exact requirements.
- **Fixed 380mA USB charge current** prevents exceeding USB max charge current.

The ISL9214 allows the flexibility to use either fast-charging rates of an AC adapter or the convenience of a USB charger.

Cradle Input: The max input voltage tolerance is 28V, programmable end-of-charge current, and the included end-of-charge latch is the default input source.

USB Input: Takes input from USB port or other low-voltage supply, fixed charge current at typically 380mA, and only charges when cradle source is not connected.

End-of-charge indicator is latched, based on completed charge.

When the battery voltage falls below minimum spec, the charger operates with a trickle charge current of 14% of the programmed cradle input or at 53mA for USB power.

Go to **www.intersil.com** for samples, datasheets and support

Intersil – Switching Regulators for precise power delivery.

intersil®
HIGH PERFORMANCE ANALOG

KYMBERLY CHRISTMAN (SCHMIDT) • MAXIM INTEGRATED PRODUCTS

Testing your notebook design for audio fidelity

THE WINDOWS LOGO PROGRAM FOR THE VISTA OPERATING SYSTEM HAS INTRODUCED NEW AUDIO-FIDELITY REQUIREMENTS FOR NOTEBOOK PCs. CRITICAL TROUBLESHOOTING TECHNIQUES CAN HELP YOU ACHIEVE COMPLIANCE.

As of June 1, 2007, the WLP (Windows Logo Program) began to impose detailed requirements on the audio performance of PCs and notebook computers using the Windows Vista operating system. The parameters in question, which the entire internal audio-signal path affects, include THD+N (total harmonic distortion plus noise), dynamic range, and crosstalk, among others. **Table 1** outlines Revision 3.09 of these playback requirements for the premium mobile class of computers.

The most noteworthy aspect of these requirements is that the industry is enforcing them. Microsoft's (www.microsoft.com) DTM (device-test manager) currently enforces a subset of the Microsoft Vista audio-fidelity requirements. The DTM Studio host computer provides an interface to the DTM-test program and test results (**Figure 1**). The system under test connects to a 2700 Series dual-domain audio analyzer from Audio Precision (www.audioprecision.com), which in turn connects to the Audio Precision host. The DTM controller controls all components via a network.

The audio analyzer can measure electrical performance only at the output jacks available on the system under test. Therefore, no one can enforce the speaker performance because the speaker is enclosed within the notebook PC box. Microsoft may soon change the DTM-test setup to accommodate acoustic-test capability, but, in the meantime, the WLP measures electrical performance only for readily accessible outputs, such as the headphone- and line-output sockets.

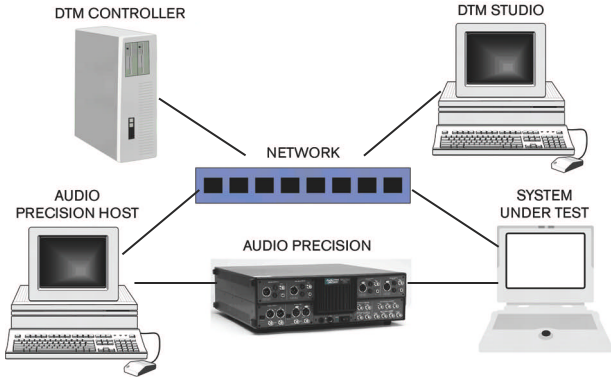


Figure 1 Microsoft's DTM (device-test manager) enforces a subset of device requirements for the WLP (Windows Logo Program). Microsoft will add additional performance tests to the DTM in the future.

Tests at the headphone-output jack validate the entire audio-signal path. System designers must therefore take care in selecting all active and passive components in that path. The audio-signal path in notebook computers and PCs begins at the south bridge, which is a motherboard chip that supports lower-speed PC functions, such as audio. The north-bridge chip supports memory and graphics. The south bridge provides an interface with the HDA (high-definition-audio) codec, which in turn feeds an analog signal to the audio amplifier in playback mode. The output of the HDA codec requires input coupling capacitors, because it can have a dc-bias voltage different from that of the audio-amplifier inputs.

Between the audio-amplifier outputs and the output jack, you may find a small EMC (electromagnetic-compatibility) filter, consisting of an inexpensive ferrite bead and a low-value ceramic capacitor (**Figure 2**). You can eliminate the large dc-blocking capacitor in the signal path of traditional audio channels by selecting a stereo-headphone amplifier, such as the MAX9724A or MAX9789A from Maxim (www.maxim-ic.com). The MAX9789A includes a speaker amplifier, headphone amplifier, and low-dropout regulator. Those devices feature Maxim's patented DirectDrive technology, which reduces the size and cost of a system by removing the need for bulky coupling capacitors.

Removing the capacitors also improves audio quality, because the piezoelectric effect of capacitors can add small amounts of distortion in the audio path. What's more, charge buildup in the capacitors often causes annoying clicks and pops at the output when you exercise power or shutdown. To avoid these problems, remove the capacitors and install the MAX9789A, which includes a 2W Class AB stereo-speaker amplifier, DirectDrive capless stereo-headphone amplifiers, and a low-dropout regulator to power the analog portion of the HDA codec, whose typical PSRR (power-supply-rejection-ratio) performance is poor. Audio quality at the MAX9789A headphone amplifiers exceeds requirements of the Vista operating system (**Table 2**).

THD+N

The first audio specification that the DTM monitors is THD+N, which quantifies the amount of nonlinearity present in a system, in the broad sense that nonlinearities are any audio-output components that are not part of the original in-

TABLE 1 WLP REQUIREMENTS AT THE ANALOG-OUTPUT JACK FOR PREMIUM MOBILE DEVICES

Device type	Requirement	Value	Frequency range
Analog-line-output jack	THD+N	≤ −65 dBFS	20 Hz to 20 kHz
	Dynamic range with signal present	≤ −80 dBFS A-weight	20 Hz to 20 kHz
	Magnitude response	≤ ±0.25-dB-ripple (0.5 dB p-p delta), 1 dB at upper-band edge, 3 dB at lower-band edge	20 Hz to 20 kHz
	Sampling-frequency accuracy	0.02%	
	Line-output crosstalk	≤ −50 dB	20 Hz to 15 kHz
	Full-scale output voltage	≥0.707V rms	
	Noise level during system activity	≤ −80 dBFS A-weight	
	Interchannel phase delay	30° or 12.5 µsec, whichever is greater	20 Hz to 20 kHz
Analog-headphone-output jack	THD+N	≤ −65 dBFS ≤ −45 dBFS at 32Ω	100 Hz to 20 kHz
	Dynamic range with signal present	≤ −80 dBFS A-weight ≤ −60 dBFS at 32Ω	100 Hz to 20 kHz
	Magnitude response	≤ ±0.25-dB-ripple (0.5 dB p-p delta), 1 dB at upper-band edge, 3 dB at lower-band edge	100 Hz to 20 kHz
	Sampling frequency accuracy	0.02%	
	Line output crosstalk	≤ −50 dB	20 Hz to 15 kHz
	Full-scale output voltage	≥0.707V rms at 320Ω, ≥300 mV rms at 32Ω	
	Noise level during system activity	≤ −80 dBFS A-weight	
	Interchannel phase delay	30° or 12.5 µsec, whichever is greater	20 Hz to 20 kHz

Note: Microsoft's Web site contains a complete listing of WLP-device requirements.

put signal. Harmonic distortion tends to color the audio signal, making it sound unnatural. Noise is the residual low-level hiss or hum that you hear in quiet periods of the audio soundtrack. Thus, a THD+N measurement is important to end users because it quantifies the level of precision to which a system reproduces an audio signal.

The THD+N measurement is a ratio of the sum of harmonics and noise (with the amplitude of the fundamental frequency removed) to the fundamental. You can express it as a percentage or in decibels referenced to an amplitude. WLP, for instance, defines THD+N in units of dBFS (decibels full-scale). **Figure 3** shows the THD+N measurement in an audio analyzer. The voltage at M2 is the sum of the harmonics plus noise, minus the amplitude of the fundamental frequency, and the voltage at M1 is the amplitude of the fundamental frequency only. To produce a graph of THD+N versus frequency, the analyzer repeatedly makes this measurement as its sinusoidal input sweeps over the audio-frequency range.

Three main factors contribute to a THD+N failure. First are the active components, which include the HDA codec or the audio amplifier. Second are the passive components, including capacitors and ferrite beads, and third is the layout,

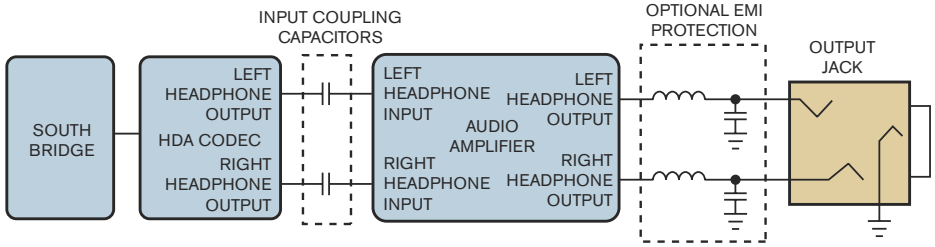


Figure 2 The Microsoft DTM measures electrical performance of the entire signal path for the headphone amplifier.

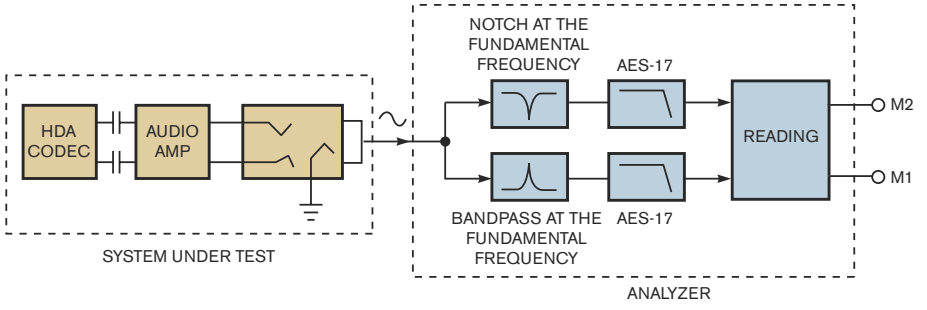


Figure 3 THD+N is the ratio of the amplitude at M2 referenced to the amplitude at M1, represented in log scale: THD+N (dBrA)=$20\times\log(V_{M2(RMS)}/V_{M1(RMS)})$. The drawing shows the bandpass filter at the fundamental frequency for conceptual reasons. Some analyzers may not use this block in the THD+N measurement.

TABLE 2 WLP REQUIREMENTS FOR PREMIUM MOBILE DEVICES VERSUS MAX9789A SPECS

Device type	Requirement	Windows Premium Mobile Vista specifications	MAX9789A/MAX9790A specifications
Analog-line-output jack, R_L=10 kΩ	THD+N	≤ – 65 dBFS	– 94 dBFS (20 Hz to 20 kHz)
	Dynamic range with signal present	≤ – 80 dBFS A-weighted	– 97 dBFS A-weighted
	Line-output crosstalk	≤ – 50 dB (20 Hz to 15 kHz)	– 77 dB (20 Hz to 15 kHz)
Analog-headphone-output jack, R_L=32Ω	THD+N	≤ – 45 dBFS (100 Hz to 20 kHz)	– 77 dBFS (20 Hz to 20 kHz)
	Dynamic range with signal present	≤ – 60 dBFS A-weighted	– 89 dBFS A-weighted
	Headphone-output crosstalk	≤ – 50 dB (20 Hz to 15 kHz)	– 74 dB (20 Hz to 15 kHz)

Note: THD+N, dynamic range, and crosstalk are measured in accordance with AES-17 audio-measurement standards.

which almost always focuses attention on grounding practices. Given a graph of THD+N versus frequency, you can easily identify one of these contributors as the root cause of failure by noting characteristics in the graph.

In general, the THD+N performance of active components degrades at high frequencies. For failures that an active component causes, therefore, the component's THD+N curve typically fails only at high frequencies. Notice that THD+N is expressed in units of dBrA, where A is defined as 1V rms (system full-scale output voltage) at the audio analyzer. If THD+N fails only at high frequencies (**Figure 4a**), turn to the component's evaluation kit, which the semiconductor vendor supplies, and evaluate the component to obtain a baseline measurement. This exercise may reveal that the selected active component is not Vista- or WLP-compliant. If it fails the Vista requirements for THD+N, you should use one of the latest Vista-compliant amplifiers, such as the MAX9789A from Maxim.

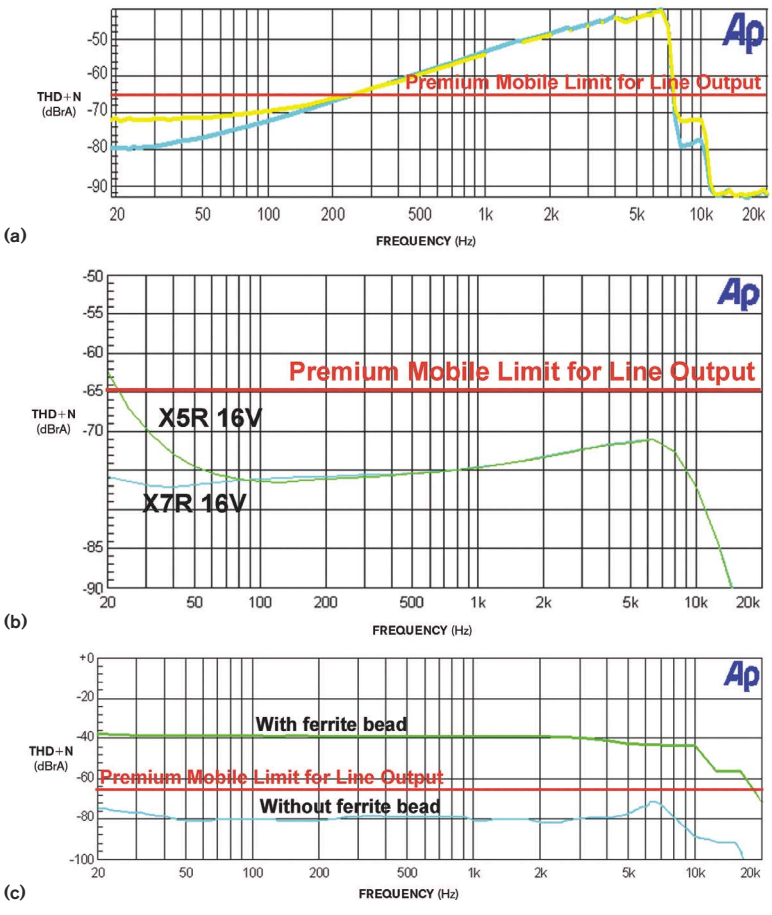


Figure 4 THD+N is recorded at constant output amplitude as you sweep the input-signal frequency from 20 Hz to 20 kHz (a). The piezoelectric effect of the input coupling capacitors can contribute signal-path nonlinearities prominent at low frequencies (b). Ferrite beads inline with the audio-signal path can increase THD (c).

A THD+N failure at only low frequencies typically points to the quality and physical size of the input coupling capacitor. In **Figure 4b**, notice how the curve for X5R dielectric begins to rise at approximately 100 Hz, whereas the X7R dielectric remains relatively flat down to 20 Hz.

The piezoelectric effect of the input coupling capacitors can contribute nonlinearities in the signal path that are prominent at low frequencies. To minimize the THD that piezoelectric action causes, choose input coupling capacitors with a higher voltage rating and better dielectric. If you require a ceramic input coupling capacitor, for example, select one with a high voltage rating and an X7R dielectric.

Ferrite beads are other passive components inline with the audio-signal path that can increase THD. If a system fails THD+N across the entire audio band, a typical cause is the quality of the ferrite bead. Notice in **Figure 4c** that the green curve with the ferrite bead, which represents a low-quality ferrite bead in series with the audio path, is almost an upward translation of the blue curve without the ferrite bead.

You typically insert ferrite beads between the audio amplifier and the output jack. In conjunction with a small capacitor to ground, the bead then forms a filter for ESD (electrostatic-discharge) or EMI (electromagnetic-interference) protection. If a system that fails THD+N

across the entire audio band includes this optional EMI-protection circuit, temporarily replace the ferrite bead with a 0Ω resistor and remeasure the THD+N. Most likely, THD+N will improve across the audio band and confirm ferrite beads as the cause of failure. **Table 3** lists ferrite beads compliant with the Vista requirements for premium mobile devices. All have been tested in-circuit for THD+N.

TABLE 3 COMPLIANT FERRITE BEADS

Manufacturer	Part no.
Murata	BLM18BD601SN1
TDK	MMZ1608Y601BTA
Taiyo Yuden	LFBK1608HM601

If active components in the system under test are Vista-compliant and you use high-quality passive components in the signal path, then layout is the most likely cause of failure. In that case, noise, rather than distortion, usually dominates the THD+N measurement. A simple FFT (fast-Fourier-transform) plot can confirm that presumption.

If noise dominates the THD+N measurement, the most likely culprit is the grounding of the HDA codec and audio amplifier. To ensure optimum performance, you must reference the codec's analog ground to the same quiet ground as that of the audio amplifier. Any difference in these ground potentials can add noise to the signal path. Reference the two analog grounds to each other, such that any movement at the codec output also appears at the input of the audio amplifier, thus producing a net voltage difference of 0V.

To avoid grounding issues, invest time upfront to map a floorplan of the PCB (printed-circuit board). Ensure that you position the analog portion of the HDA codec close to the analog portion of the audio amplifier. Also ensure that the headphone ground return does not pass through sensitive analog circuitry. These simple precautions can reduce or eliminate headaches later in the design cycle.

FULL-SCALE OUTPUT VOLTAGE

The DTM also monitors full-scale output voltage, which is the voltage level you measure at the output jack when you configure the codec with all zeros. The DTM specifies a minimum voltage at the output jack for WLP devices. Full-scale voltage is important, because it ensures that the end user can, for example, comfortably listen to DVDs in a noisy environment, such as on an airplane.

To avoid lawsuits based on hearing damage, the industry recently set restrictions on the upper limit of this specification. You should therefore keep in mind that a maximum output-voltage specification may accompany the minimum output-voltage specification, especially for products manufacturers ship to France or Germany.

If a system fails the output-voltage specification, its signal path includes some source of attenuation. Such attenuation can occur in the codec output, the audio-amplifier output, or the output jack (**Figure 5**). You can easily confirm a problem in the codec or codec driver by probing between the codec's HDA outputs and the input coupling capacitors. If an oscilloscope does not show a full-scale signal at that point, the problem is most likely in the codec driver.

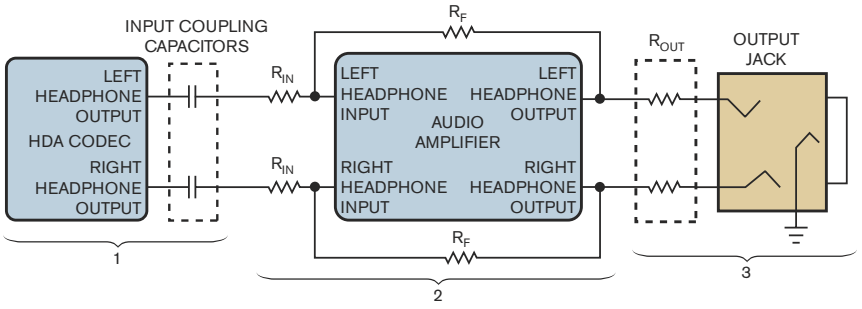


Figure 5 You can partition the headphone amplifier's signal path into three sections when troubleshooting failures of the full-scale output voltage.

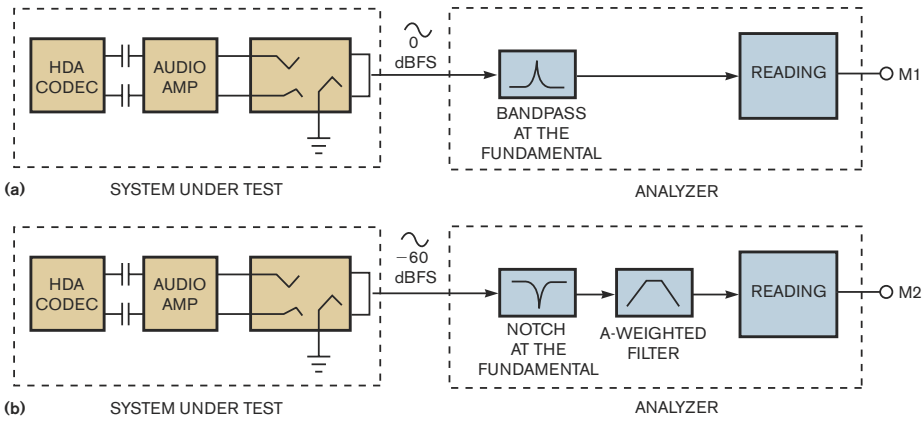


Figure 6 Dynamic range is the ratio of full-scale output voltage to the weighted rms-noise floor: Dynamic range (dB)=20×log($V_{M2(RMS)}$/$V_{M1(RMS)}$) (a). You measure the noise floor in the presence of a −60-dBFS signal, which you then notch out of the noise-floor measurement (b).

Next, inspect the audio-amplifier output. An improperly configured external gain for the audio amplifier may account for the output attenuation. To check the external gain, you should confirm that the feedback resistance is greater than or equal to the input resistance.

Now, examine the output jack. If you measure full-scale output voltages at the first two locations but a reduced signal at the output jack, you most likely have inserted series resistors between the audio amplifier and the output jack. Series resistors form a voltage divider with the load at the output jack, so testing with a 32Ω load rather than a 10-kΩ load exagger-

ates the attenuation effect. To remove the attenuation, replace the series resistors with 0Ω resistors.

DYNAMIC RANGE

Dynamic range is another audio specification that the DTM electrically monitors. Dynamic range with signal present is the ratio of the weighted-rms-noise floor over the full-scale reference level. You record the weighted-noise-floor measurement in the presence of a −60-dBFS signal and then you notch out the −60-dBFS signal from the analyzer's dynamic-range reading.

Figure 6 shows the dynamic-range measurement in an audio analyzer. Dynamic range is the ratio of the weighted-rms-noise floor over the full-scale output. The voltage at M1 is the full-scale output voltage measured at the output jack, and the voltage at M2 is the weighted-rms-noise floor, minus the fundamental frequency of the −60-dBFS test signal. You express the units in decibels.

The two main contributors to a dynamic-range failure are attenuated output level and elevated noise floor. If a system's full-scale output voltage is acceptable, the system is halfway to Vista compliance in dynamic range. First, confirm that the output-jack voltage meets the full-scale requirement. If not, determine where attenuation occurs in the signal path.

If the system reproduces a full-scale signal at the output jack, noise limits the dynamic-range measurement. Before troubleshooting the noise source, confirm that active components in the system are Vista-compliant with respect to noise.

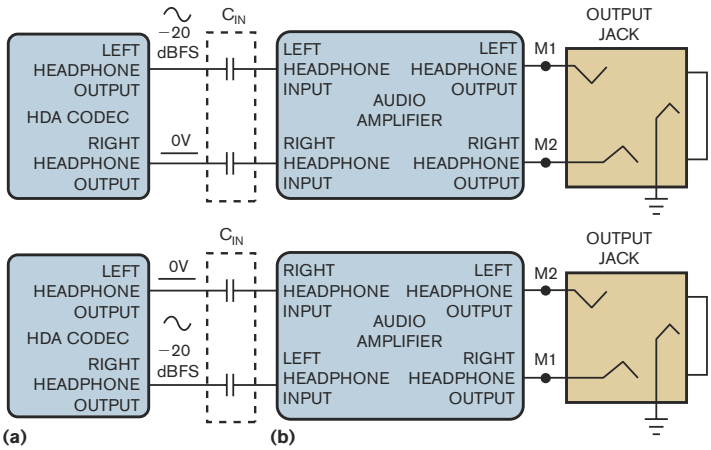


Figure 7 Crosstalk from the left channel to the right channel is the ratio of the signal measured on the right channel (a) over the signal measured on the left channel (b): Crosstalk (dB)=20×log($V_{M2(RMS)}$/$V_{M1(RMS)}$).

(You can usually find this specification in the electrical-characteristics table of the device's data sheet.) Otherwise, turn to evaluation kits for the active devices, and record baseline measurements.

If noise dominates the system's dynamic-range measurement and its active components are Vista-compliant, the PCB layout is usually to blame. The main pitfall in layout is the grounding. To ensure optimum performance, reference the analog ground of the HDA codec to the same quiet ground as

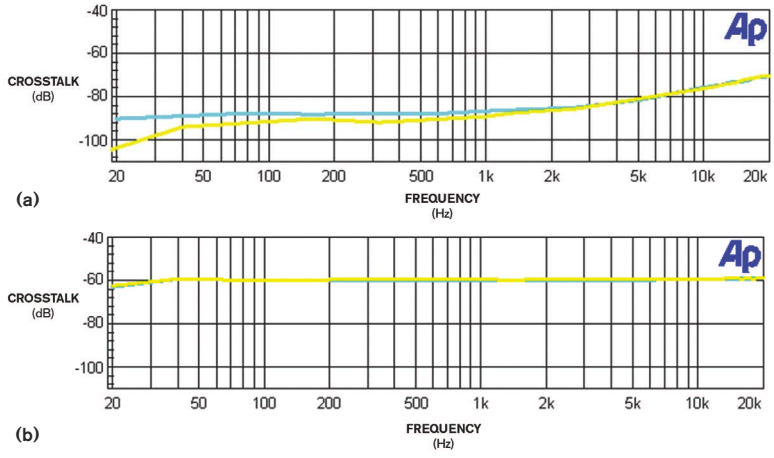


Figure 8 If a crosstalk measurement produces a positive slope as you sweep the frequency from 20 Hz to 20 kHz, the system most likely has capacitive coupling at the inputs of the audio amplifier (a). If the system has a shared resistive ground return, the crosstalk measurement is relatively flat across the audio band (b).

the audio amplifier. A difference in these ground potentials can add noise to the signal path.

If, after optimizing IC placement to achieve a common, quiet analog ground for the HDA codec and audio amplifier, you achieve no improvement, you must work further to isolate the noise source. First, confirm that system noise, including fan noise, hard-disk-drive noise, and other contributors, is not coupling into the amplifier inputs. If such noise is present, the audio amplifier can amplify it and pass it to the output jack. Second, confirm whether you have referenced the ground pin of the output jack to the same analog ground as the analog portion of the HDA codec and audio amplifier. Again, a difference in these ground potentials can add noise to your signal path.

CROSSTALK

Crosstalk is an audio specification that the DTM does not yet enforce, but it is likely to do so in the near future. Crosstalk quantifies the amount of signal that couples from one channel to another. An ideal stereo-signal path would have no crosstalk between channels, but parasitics in the IC and PCB layouts guarantee some minimum level of crosstalk. You must minimize crosstalk to ensure a true stereo image at the outputs.

Two conditions define stereo crosstalk: from left channel to right channel and from right channel to left channel. A measurement from left to right takes the ratio of the signal measured on the right channel over the signal measured on the left channel (**Figure 7**). During this measurement, the signal on the right channel is 0V, and the left-channel input of −20 dBFS sweeps across the audio band. You express the

crosstalk measurement in decibels.

The top contributor to crosstalk failures is layout, whether of the IC or the PCB. Given the crosstalk limits of WLP 3.0—≤−50 dB between 20 Hz and 15 kHz—a crosstalk failure is rarely due to the IC layout. Maxim's MAX9789A, for example, has a crosstalk specification of ≤−77 dB into a 10-kΩ load, across the entire audio band. (It's always a good idea, however, to confirm the baseline-crosstalk measurement using an evaluation kit for the active component.) The main cause of crosstalk failure is almost always the PCB layout: either capacitive coupling between the inputs or a shared resistive ground return at the output jack.

MORE AT EDN.COM

Go to www.edn.com/ms4282 and click on Feedback Loop to post a comment on this article.

If a crosstalk measurement has a positive slope as you sweep frequency from 20 Hz to 15 kHz, the system has capacitive coupling at the audio-amplifier inputs (**Figure 8a**). Capacitive coupling becomes apparent when you apply a high-impedance drive at the audio-amplifier inputs. The high impedance can originate in an improperly configured codec driver. You should therefore be sure to configure the HDA-codec outputs for a 1 to 2Ω output drive. Otherwise, you can configure the codec for a low-impedance drive state.

If external resistors set the amplifier gain, ensure that the series resistor, R_{IN}, is as close as possible to the amplifier inputs, so that a low-impedance source drives the amplifier. If you configure the system for low-impedance drive and its crosstalk measurement still fails at 15 kHz, you may have routed the stereo inputs too close together. To provide optimum stereo separation, insert a solid ground fill between the amplifier inputs.

If the crosstalk measurement is relatively flat across the audio band yet fails the crosstalk specification, the typical cause is a shared resistive-ground return (**Figure 8b**). Avoid a shared return by ensuring minimal resistance in the return path for the output jack's ground connection. Short out any series resistors in the path, locate audio amplifiers close to the output jack to minimize the length of the ground return, and minimize contact resistance to the sleeve of the output jack itself. These concepts also apply to the ground-return path to the HDA codec.

MAGNITUDE RESPONSE

The WLP also specifies criteria for the magnitude response. Magnitude response is a measurement of the system's output voltage over a given frequency range. You typically reference this response to the system's full-scale signal level and express it in decibels. Magnitude response is important because it specifies the audio bandwidth the system can reproduce.

You measure magnitude response by sweeping a constant-amplitude pure tone of −20 dBFS through the audio bandwidth. You measure the output level relative to the output level at 997 Hz.

The system's equalization circuitry, which can cause inaccurate-response measurements by boosting or suppressing certain frequencies within the measurement bandwidth, can cause a failure in magnitude response. When measuring a system for

magnitude response, be sure to disable the system-equalization circuitry.

Other possible causes of magnitude-response failure are the passive components, which can form a filter that affects high or low frequencies. If the system fails at high frequencies, confirm that any feedback capacitors around the headphone amplifier are not limiting the magnitude response. The feedback resistors, too, can cause unanticipated attenuation in the audio bandwidth. A simple $1/(2\pi RC)$ calculation can reveal whether this is the case. Remember to account for tolerance in the passive-component values.

If the system fails at low frequencies and your headphone amplifier requires large dc-blocking capacitors at the output, select an output-capacitor value that ensures that the system is Vista-compliant for both 32Ω and 10-kΩ loads. Again, be sure to account for tolerance in the value of the dc-blocking capacitor.

If the system fails at low frequencies even though its headphone amplifier does not require dc-blocking capacitors before the output jack, as is the case with Maxim's MAX9724A, for instance, check that the values of the input coupling capacitors are Vista-compliant. And remember to account for tolerance when selecting values for the input coupling capacitors and resistors.

INTERCHANNEL-PHASE DELAY

Interchannel-phase delay is a Vista specification that Microsoft only recently added to the DTM program. For stereo devices, it is the measured phase difference between left and right channels, which you express in degrees or microseconds as a function of frequency. You obtain interchannel phase delay by measuring the relative phase difference between the stereo-audio outputs while sweeping the audio signal from 20 Hz to 20 kHz.

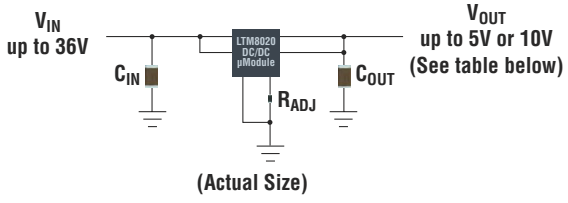
If a system fails the requirements for interchannel-phase delay, there may be an insufficiently tight tolerance on the passive-component values inline with the stereo channels. There may be a mismatch, for example, in values for the left- and right-channel input coupling capacitors. If, on the other hand, the passive components have sufficiently tight tolerances, there may be something wrong in the digital domain. Some system block within the active component may be functioning improperly.

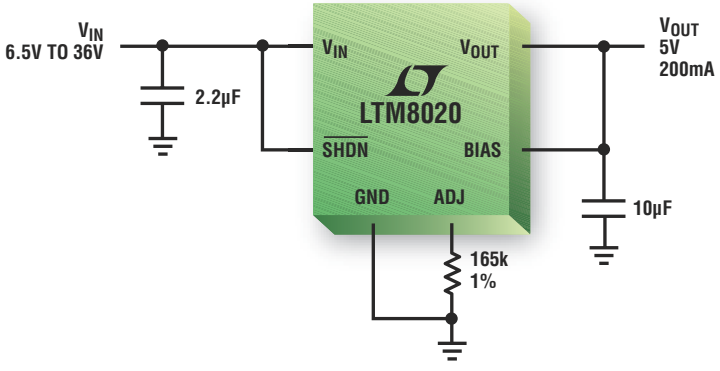
To help you with Vista-compliance troubleshooting, Maxim has generated an online tool that presents system engineers with a decision tree for determining the cause of system failures. Find it at www.maxim-ic.com/fidelity-debug-tool. EDN

AUTHOR BIOGRAPHY

Kymberly Christman (Schmidt) is a corporate applications engineer at Maxim Integrated Products, specializing in audio-design support and product definition for the multimedia-business unit. She has a bachelor's degree in electrical engineering from the University of California—Los Angeles.

36V_{IN} µModule DC/DC Family





Compact, Low Profile & No Heat Sink

Our new DC/DC µModule™ regulators with up to 36V_{IN}, 200mA to 2A, operate cooler than linear regulators and are simpler than discrete switchmode DC/DC regulators. With onboard inductor, power switches and other circuitry, the LTM®8020, LTM8021, LTM8022 and LTM8023 are complete switchmode DC/DC regulator systems in an IC form factor. Low profile, thermally efficient and compact, they mount on either side of the board, leaving space for digital ICs.

Features

- Onboard inductor, power components, DC/DC regulator, input/output bypass capacitors and compensation circuitry
- Current mode operation for fast short-circuit response, accurate current limiting and precise line and load regulation
- LGA package with gold finished pads allow soldering with Pb and Pb-free solder pastes
- RoHS compliant
- Simple copy-and-paste layout

The New 200mA to 2A DC/DC µModule Family

	LTM8020	LTM8021	LTM8022	LTM8023
V_{IN}	4V to 36V	3V to 36V	3.6V to 36V	3.6V to 36V
V_{OUT}	1.25V to 5V	0.8V to 5V	0.8V to 10V	0.8V to 10V
I_{OUT}	200mA	500mA	1A	2A
Size (mm)	6.25 x 6.25 x 2.3	6.25 x 11.25 x 2.8	11.25 x 9 x 2.8 Pin Compatible	

More Info

www.linear.com/micromodule

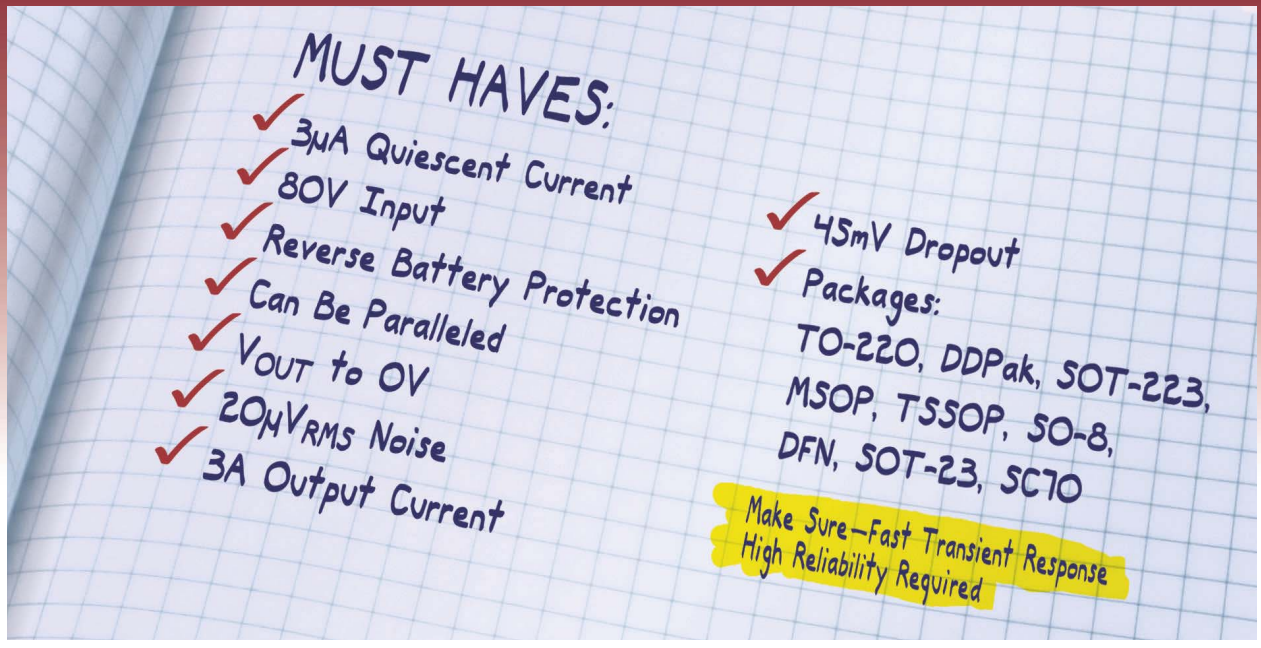
1-800-4-LINEAR

Free DC/DC Telecom, Datacom and Industrial Brochure

www.linear.com/48vsolutions

LINEAR TECHNOLOGY

High Performance LDOs



A new generation of high performance LDOs is now available from Linear. These LDOs are a generation beyond previous regulators in feature benefits and performance. These include ultralow quiescent currents to maximize battery life, low output noise to minimize potential interference, high input voltages for increased flexibility, protection features for rugged designs and an array of package options to facilitate both leaded and surface mount requirements.

High Performance, Low-Noise LDOs

Part No.	I_{OUT}	Max. V_{IN} (V)	Dropout Voltage (V)	Noise (μV_{RMS})	I_Q	Output Voltage (V)	Package (mm)
LT®3009	20mA	20	0.28	150	3µA	Adj. (0.6 to 19.5)	2 x 2 DFN-6, SC70-8
LT3010/H*	50mA/50mA	80	0.30	100	30µA	Adj. (1.275 to 60), 5	ThinSOT™
LT1761	100mA	20	0.30	20	20µA	Adj. (1.22 to 20), Fixed	ThinSOT
LT1762	150mA	6.5	0.30	20	25µA	Adj. (1.22 to 20), Fixed	MSOP-8
LT3012/H*	250mA/200mA	80	0.40	100	40µA	Adj. (1.24 to 60)	3 x 4 DFN-12, TSSOP-16E
LT3013/H*	250mA/200mA	80	0.40	100	65µA	Adj. (1.24 to 60)	3 x 4 DFN-12, TSSOP-16E
LT1962	300mA	20	0.27	20	30µA	Adj. (1.22 to 20), Fixed	MSOP-8
LTC®3025	300mA	5.5	0.05	80	54µA	Adj. (0.4 to 3.6)	2 x 2 DFN-6
LTC3035	300mA	5.5	0.045	150	100µA	Adj. (0.4 to 3.6), Fixed	2 x 2 DFN-6
LT1763	500mA	20	0.30	20	30µA	Adj. (1.22 to 20), Fixed	SOIC-8
LTC3025-1/-2	500mA	5.5	0.075	80	54µA	Adj. (0.4 to 3.6)/1.2	2 x 2 DFN-6
LT3080**	1.1A***	36 (40 Abs Max)	0.3+	40	1mA	Adj. (0 to 36)++	3 x 3 DFN-8, MSOP-8E, TO-220, SOT-223
LT1965	1.1A	20	0.29	40	500µA	Adj. (1.20 to 19.5)	3 x 3 DFN-8, MSOP-8E, TO-220, DDPak
LT1963/A	1.5A	20	0.34	40	1mA	Adj. (1.21 to 20), Fixed	DDPak, TO-220, SOT-223, SO-8
LT1764/A	3A	20	0.34	40	1mA	Adj. (1.21 to 20), Fixed	DDPak, TO-220

*Tj = 140°C Operation (H-grade)
**Current-based Reference
***Can Be Paralleled
+Two-supply Operation
++Single-resistor V_{OUT} Set

Info & Free Samples

www.linear.com/LDOs

1-800-4-LINEAR

Free Portable Solutions Brochure

www.linear.com/portsolutions

LINEAR TECHNOLOGY

EDITED BY CHARLES H SMALL
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Small capacitor supports telecom power supply during brownouts

Samuel Kerem, Rockville, MD

This Design Idea shows how to keep telecom equipment operational during a short brownout. You must first understand a few details regarding the power supply for telecom equipment. The common voltage of the power source that feeds telecom equipment is −48V, although the actual voltage can range from −42.5 to −56V, −40 to −60V, or even beyond. The common power-"brick" dc/dc converter operates over the −36 to −75V range. A brownout occurs when the −48V source drops to 0V and stays there as long as 10 msec.

Using capacitive storage that connects to the brick's input is an obvious approach to overcoming this problem, but a shortcoming becomes apparent when you understand the reality of the −48V supply. For example the energy in a capacitor charged to voltage is $(C \times V^2)/2$, where C is the capacitance and V is the voltage. The brick stops its operation when the capacitor discharges to 36V. In general, the energy available to support the brick's operation is, therefore:

$$U = C \times \frac{\left(V_1^2 - V_2^2\right)}{2},$$

where V_1 and V_2 are the beginning and final −36V voltages, respectively, and U is the energy. Also, $U = P \times t$, where P is power and t is time. Using these equations, you can find the time that the equipment will stay operational:

$$t = C \times \frac{\left(V_1^2 - V_2^2\right)}{2 \times P},$$

or, to define the capacitor's value:

$$C = \frac{2 \times P \times t}{V_1^2 - V_2^2}.$$

Assume that the brownout occurs when the voltage at the brick's input is −39V, which is the case when −48V is −40V but the brick loses at least 1V because of protective ORed diodes in a hot-swap configuration. Also, assume that the storage capacitor charges to −39V. The equipment operates until this storage capacitor discharges to −36V. Assume that the equipment consumes 100W. To store enough energy for 5 msec, the capacitor's value would have to be approximately 4500 µF. The capacitor must be rated for the maximum possible incoming voltage, which can be more than 75V, so the minimum rating of 100V is a must. The 4500-µF, 100V capacitor is a sizable part. If the design requires twice as much operational time at a power consumption of 300W, the capacitor must have a value of 27,000 µF and 100V.

This Design Idea still requires a capacitor, but the capacitor has a lower value—that is, 200 µF versus 4500 µF—and sustains 100W during a 5-msec brownout. This approach increases reliability and reduces cost and size. The hidden feature is the power brick's ability to stay operational over the input range of −36 to −75V and even to operate under surges greater than

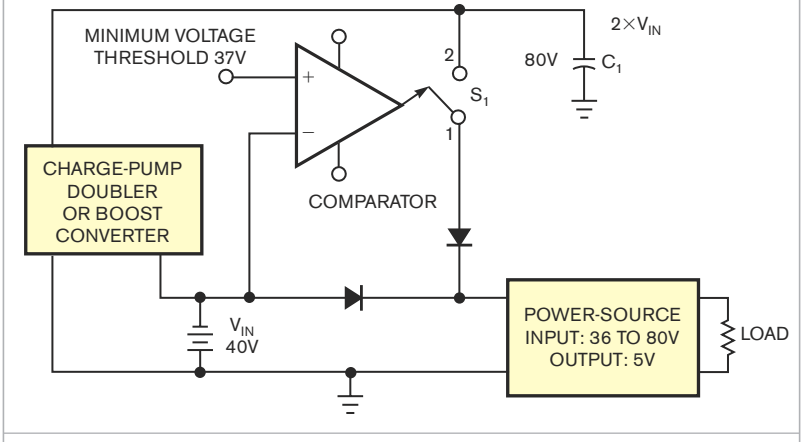


Figure 1 Charged to double the input voltage, the energy stored in capacitor C_1 dumps into the input of the "brick" power supply during brownouts when the input voltage drops to less than −37V.

DIs Inside

▶What are your design problems and solutions? Publish them here and receive $150! Send your Design Ideas to edndesignideas@reedbusiness.com.

−80V. **Figure 1** shows how you can use this feature. The **figure** depicts a positive input voltage. The brick is isolated, so polarity is irrelevant, but positive interpretation is easier to illustrate.

Remember that the stored energy in the capacitor grows exponentially, whereas the capacitor's voltage increases linearly. The doubler charges C_1 to twice the input voltage or at least to 80V. Even if, hypothetically, you expect a 5-msec brownout as often as 10 sec, the current to charge 200 µF is still only approximately 3 mA. The comparator watches the input voltage, and, as soon as it drops below 37V, switch S_1 closes, and the energy from C_1 discharges to the power brick. EDN

Tiny microcontroller hosts dual dc/dc-boost converters

Dhananjay V Gadre, Netaji Subhas Institute of Technology, New Delhi, India

Batteries are the typical power sources for portable-system applications, and it is not unusual these days to find microcontroller-based portable systems. A variety of microcontrollers operates at low power-supply voltages, such as 1.8V. Thus you can employ two AA or AAA cells to power the circuit. However, if the circuit requires higher voltage—for LED backlighting for an LCD, for example, which requires approximately 7.5V dc—you must employ a suitable dc/dc converter to boost the power-supply voltage from, for example, 3V to the required voltage. However, you can also employ a microcontroller to develop a suitable dc/dc-boost-voltage converter (**Reference 1**) with the help of a few additional discrete components.

This Design Idea shows how to create not just one, but two dc/dc converters with just a tiny eight-pin microcontroller and a few discrete components. The design is scalable, and you can adapt it for a wide range of output-voltage requirements just by changing the control software for the microcontroller. You can even program the microcontroller to generate any required output-voltage start-up rate. **Figure 1** shows the basic topology of a boost switching regulator. The output voltage in such a regulator is more than the input voltage. The boost switching regulator operates in either CCM (continuous-conduction mode) or DCM (discontinuous-conduction mode). It is easier to set up a circuit for DCM operation (**Reference 2**). The name comes from the fact that the inductor current falls to 0A for some time during each PWM period in DCM; in CCM, the inductor current is never 0A. The maximum current passes through the inductor at the end of high period of the PWM output (when the switch is on) and is:

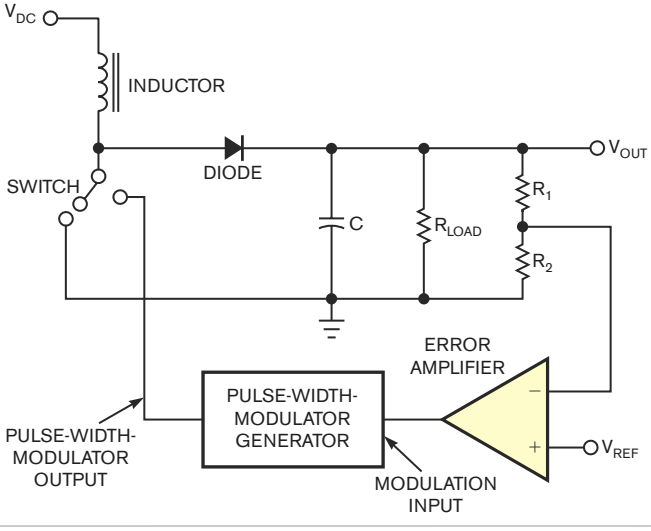


Figure 1 The output voltage in a boost switching regulator is more than the input voltage. The boost switching regulator operates in either CCM (continuous-conduction mode) or DCM (discontinuous-conduction mode)

$$I_{L_{MAX}} = \frac{V_{DC} \times D \times T}{L}, \quad (1)$$

where V_{DC} is the input voltage, D is the duty cycle, T is the total cycle time, and L is the inductance of the inductor. The current through the diode falls to zero in time T_R.

$$T_R = \frac{V_{DC} \times D \times T}{(V_{OUT} - V_{DC})}, \quad (2)$$

The load current is the average diode current,

$$I_{LOAD} = \frac{I_{L_{MAX}} \times T_R}{2 \times T}, \quad (3)$$

from **equations 1** and **2** and simplifies to:

$$I_{LOAD} = \frac{V^2_{DC} \times D^2 \times T}{2 \times L \times (V_{OUT} - V_{DC})}. \quad (4)$$

The output voltage, V_{OUT}, is:

$$V_{OUT} = V_{DC} \times \left(1 + \frac{V_{DC} \times D^2 \times T}{2 \times L \times I_{LOAD}}\right), \quad (5)$$

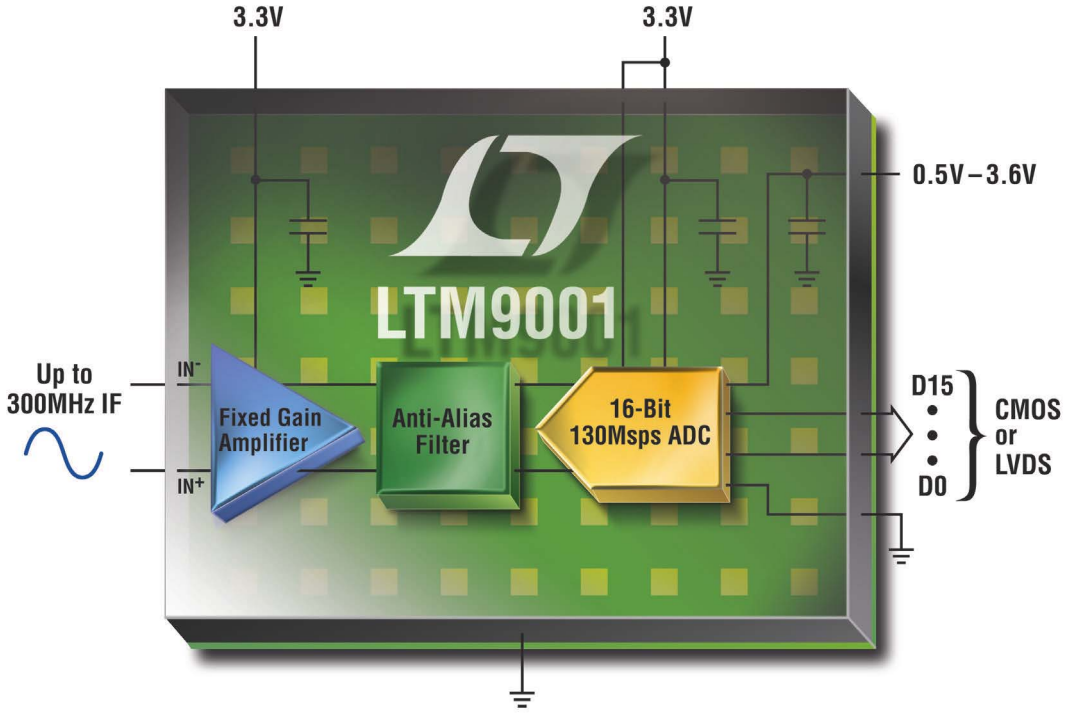
The value of the output capacitor, which determines the ripple voltage, is:

$$\frac{dV}{dt} = \frac{I}{C}. \quad (6)$$

where dV/dt represents the drop in the output voltage during the period of the PWM signal, I is the load current, and C is the required output capacitor.

The total period of the PWM wave

16-Bit, 130Msps ADC + Driver



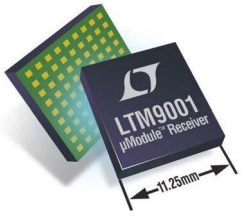
µModule™ Subsystem Dramatically Reduces Design Complexity & Board Space

The LTM®9001 is a 16-bit, 130Msps IF/baseband receiver subsystem that leverages years of applications engineering expertise to maximize high speed ADC performance. The LTM9001 alleviates the need for driver and ADC impedance matching, filtering, bypass placement and layout, eliminating long hours of troubleshooting and reducing time to market. With no external components required, the LTM9001 provides a high performance solution in less than half the board space of a discrete implementation.

Features

- Integrated 16-Bit, 130Msps ADC, Filter and Amplifier
- 72dB SNR, 82dBc SFDR @ 162.5MHz
- Up to 300MHz IF Range
- Fixed Gain: 8dB, 14dB, 20dB or 26dB
- 50Ω, 200Ω or 400Ω Input Resistance
- Integrated Bypass Capacitance, No External Components Required
- Optional Internal Dither
- Optional Data Output Randomizer
- 11.25mm x 11.25mm LGA Package

LTM9001: 16-Bit IF/Baseband Receiver Subsystem



Info & Free Samples

www.linear.com/9001

1-800-4-LINEAR

Wireless Solutions Brochure

www.linear.com/wireless

LINEAR TECHNOLOGY

is T and is a system constant. D is the duty cycle of the PWM wave, and T_R is the time during which the diode conducts. At the end of T_R, the diode current falls to 0A. The period of the wave is $T>D\times T+T_R$ for DCM. The difference of the PWM period, T, and $(D\times T+T_R)$ is the dead time.

The switch that operates the inductor is usually a BJT (bipolar-junction transistor) or a MOSFET. A MOSFET is preferable because of its ability to handle large current, better efficiency, and higher switching speed. However, at low voltages, a suitable MOSFET with low enough gate-to-source threshold voltage is hard to find and can be expensive. So, this design uses a BJT (**Figure 2**).

Microcontrollers offer PWM frequencies of 10 kHz to more than 200 kHz. A high PWM frequency is desirable because it leads to a lower inductor value, which translates to a small inductor. The Tiny13 AVR microcontroller from Atmel (www.atmel.com) has a "fast" PWM mode with a frequency of approximately 37.5 kHz and a resolution of 8 bits. A higher PWM resolution offers the ability to more closely track the desired output voltage. The maximum inductor current from **Equation 1** is 0.81A for a 20-µH inductor. The transistor that switches the inductor should have a maximum collector current greater than this value. A 2SD789 NPN transistor has a 1A collector-current limit, so it is suitable for this dc/dc converter. The maximum load current achievable with these values, from **Equation 4**, is 54 mA and thus meets the requirement of maximum required load current for an output voltage of 7.5V.

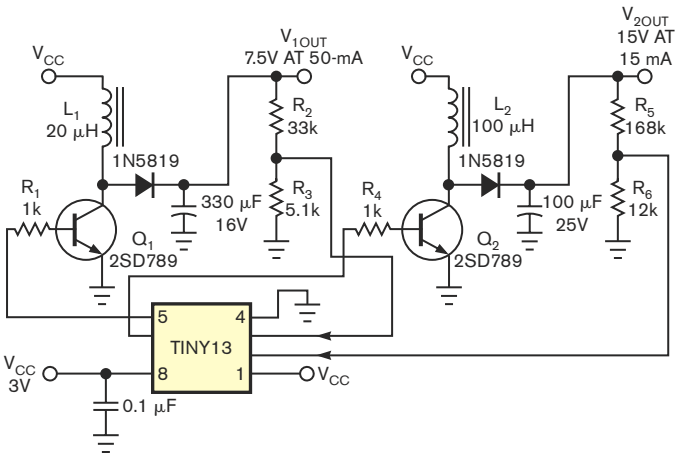


Figure 2 An Atmel Tiny13 AVR microcontroller regulates two boost-dc/dc-converter outputs using its internal ADCs and PWMs.

The Tiny13 microcontroller boasts two high-speed PWM channels and four 10-bit ADC channels. Another PWM channel and an ADC channel create the second dc/dc converter for an output voltage of 15V and a maximum load current of 15 mA. The inductor for this converter has a value of 100 µH. To calculate the output-capacitor value, use **Equation 6**. For a 5-mV ripple, the value of the capacitor for 7.5V output voltage is 270 µF, because the output current is 50 mA and the PWM-time period is 27 µsec, so this circuit uses the nearest larger value of 330 µF. Similarly, for the 15V output voltage, the required capacitor value is 81 µF, so the design uses a 100-µF capacitor.

The programs for the microcontroller are in C and use the open-source AVR GCC compiler (www.avrfreaks.net). They are available in the Web version of this Design Idea at www.edn.com/080515di1. The AVR Tiny13 microcontroller operates at an internal clock frequency of 9.6 MHz without an internal-clock-frequency divider, so the PWM frequency is 9.6 MHz/256=37.5 kHz. The internal reference voltage is 1.1V. The main program alternately reads two channels of ADCs that monitor the output voltages in an interrupt subroutine. The main program executes an endless loop, monitoring the output voltage by reading the ADC values and adjusting the PWM values accordingly. EDN

REFERENCES

1 "Boost converter," Wikipedia, http://en.wikipedia.org/wiki/Boost converter.

2 Pressman, Abraham I, *Switching Power Supply Design, Second Edition*, McGraw-Hill Professional, Nov 1, 1997, ISBN-10: 0070522367, ISBN-13: 978-0070522367.

Cross-coupled gates prevent push-pull-driver overlap

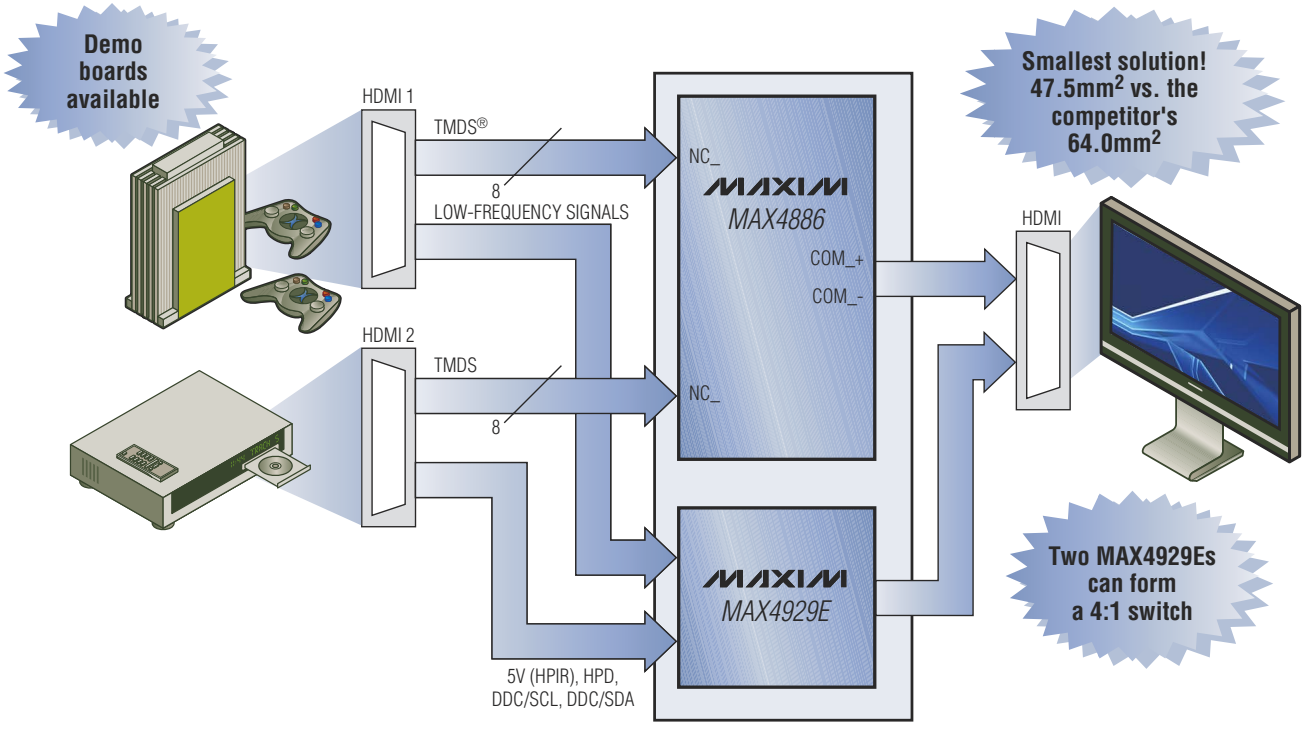
Richard Rice, Oconomowoc, WI

Overlap—the short period during which a push-pull drive's two transistors are both simultaneously on—is a common problem with these drives in a center-tapped transformer's primary. Overlap causes a large current spike and increased switching losses. The fact that saturated transistors turn off more slowly than they turn on causes the problem. One method of preventing overlap is to provide a time delay after turning off one transistor and before turning on the other one. This method requires several extra components and must include enough delay for a worst-case scenario. This Design Idea uses cross-coupled gates to prevent one transistor from turning

MAXIM 1983 • 2008 25 YEARS OF ENGINEERING SUCCESS

Industry's first ultra-broadband HDMI/DVI switches

Two-chip solution enables picture-perfect 1080p performance



HDMI™/DVI™ TMDS switch (MAX4886)

- 3.3V rail-to-rail switch
- 2.6GHz (typ) bandwidth
- 1920 x 1080 pixels
- Less than 20ps skew
- -0.6dB (typ) ultra-low insertion loss
- 3.5mm x 9.0mm, 42-pin TQFN package

Low-frequency control switch (MAX4929E)

- Integrated control: two sources to one sink
- ±15kV ESD protection* on all external I/Os
- Hot-plug detect signal matches MCU to TTL levels
- 3.0V to 5.5V DDC output clamping
- 4mm x 4mm, 20-pin TQFN or 20-pin QSOP

TMDS is a registered trademark of Silicon Image, Inc.
HDMI is a trademark of HDMI Licensing, LLC.
DVI is a trademark of Digital Display Working Group (DDWG).
*Human Body Model.

Technical Support
www.maxim-ic.com/support

MAXIM DIRECT
www.maxim-ic.com/shop

AVNET electronics marketing
www.avnet.com

MAXIM
www.maxim-ic.com/MAX4886-info

For a free sample visit www.maxim-ic.com/samples or call 1-800-998-8800

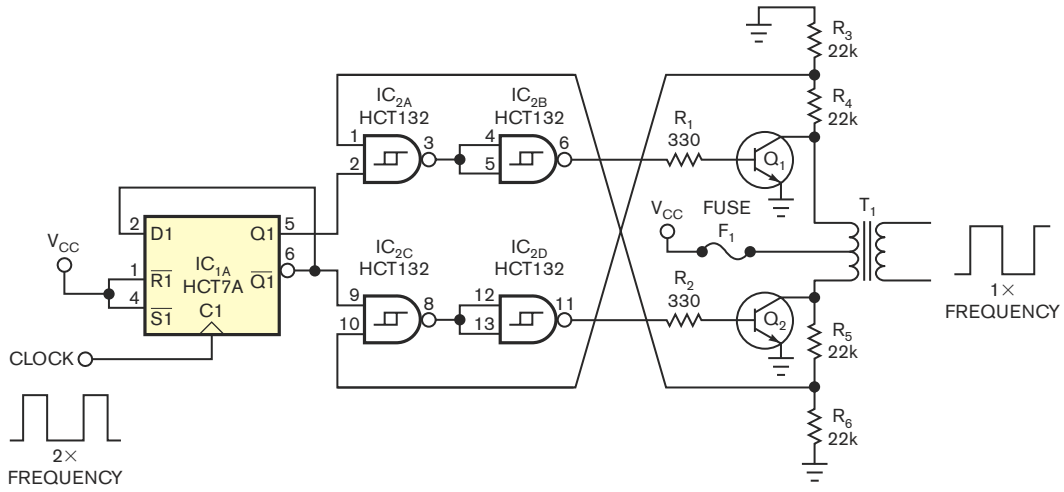


Figure 1 Cross-coupled gates prevent one transistor from turning on before the other turns off. Fuse F_1 protects against catastrophic failures.

on before the other turns off (**Figure 1**). For simplicity, the **figure** omits the depiction of bypass capacitors, snubber networks, and other components unnecessary for illustrating the method.

Gate IC_{2A} prevents Q_1 from turning on until Q_2 turns off. Likewise, gate IC_{2C} prevents Q_2 from turning on until Q_1 turns off. Gates IC_{2B} and IC_{2D} function as inverters to provide the correct polarity to drive the switching transistors. Monitoring the transistors' collector voltages senses the turn-off of each transistor using the voltage dividers R_3/R_4 and R_5/R_6. Because the collector voltage swings to twice the supply voltage, the voltage dividers halve the voltage. The impedance of the voltage dividers also limits the gates' input current to a safe level during overshoot. The switching frequency is one-half the input-clock frequency. D-type flip-flop IC_{1A} divides the input-clock frequency by two and provides complementary outputs with a 50% duty cycle. The complementary outputs drive the switching transistors in an alternating sequence. The secondary of transformer T_1 provides an isolated square-wave output. EDN

Save valuable picoseconds using ECL-wired OR

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

Often, when you are designing with high-speed ECL (emitter-coupled logic), you have too little time between clock cycles to implement logic functions using gates between flip-flops. In these cases, you can derive equivalent-logic functions using the wired-OR and flip-flop complementary inverted outputs (**references 1**, **2**, and **3**). You can parallel the emitter-follower outputs of ECL with a pulldown resistor to implement the OR function with almost no time-delay penalty. Complementary outputs—one inverted—provide delay-free logic inversions.

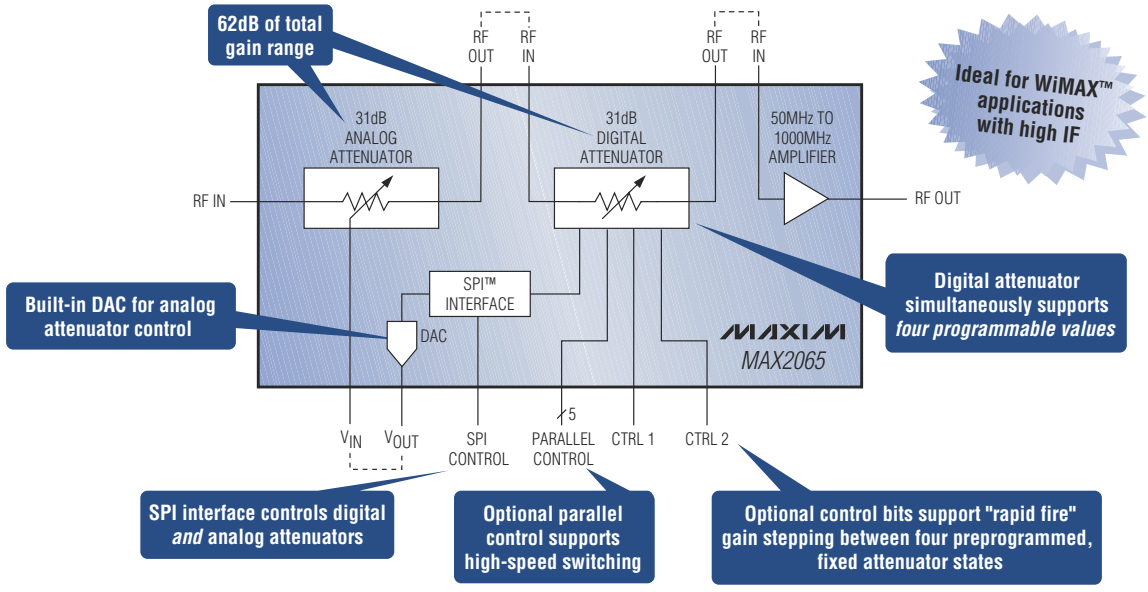
This Design Idea uses the older Motorola (www.motorola.com) 10H ECL logic family, the fastest available when I was building the design (**Figure 1**). Newer ECL families are much faster, but the same wired-OR principle applies. For clarity, the **figure** omits power and 50Ω pulldown resistors. This design needed an XOR comparison between a PRBS (pseudorandom-binary-sequence) data stream and a local PRBS reference for a BER (bit-error-rate) counter running at 250 Mbps (**Figure 1a**). A problem occurred with the design, however: The clock period at 250 Mbps is 4 nsec, whereas the 10H107 XOR/XNOR gate's maximum propagation delay is 1.7 nsec. In addition, the 10H131 flip-flop's maximum propagation delay is 1.8 nsec, and the required input-setup time is 0.7 nsec. All these delays total 4.2 nsec, which exceeds the 4-nsec clock period by 200 psec. Adding a fourth flip-flop with wired-OR outputs to replace the 10H107 XOR/XNOR solves the problem (**Figure 1d**).

The XNOR-equivalent function uses NOR, AND, and OR functions (**Figure 1b**). The circuit in **Figure 1c** separates the NOR into the equivalent OR with an output inverter and converts the AND into the equivalent OR with inverted inputs and output. Now, the circuit uses only ORs and inverters. This form is necessary for implementing the wired-OR equivalent (**Figure 1d**). In this case, the inverted-complementary outputs of the flip-flops replace the

MAXIM 1983 • 2008 25 YEARS OF ENGINEERING SUCCESS

Industry's only fully programmable, multistate, analog and digital VGAs

High-linearity monolithic solutions cover 50MHz to 1000MHz



- Excellent linearity
  - Up to +42dBm OIP3, +61dBm OIP2, +18.5dBm OP_{1dB}
  - -63dBc HD2 and -80dBc HD3 performance
- Noise figures as low as 4.2dB
- Fast, 40ns digital switching
- Very low digital VGA amplitude overshoot/undershoot
- 5V or 3.3V supply
- Supports four "rapid fire" preprogrammed attenuator states
  - Quickly access any one of four customized attenuation states without reprogramming the SPI bus
  - Ideal for fast-attack, high-level blocker protection
  - Prevents ADC overdrive condition

Part	VGA Type	Frequency (MHz)	Gain Range (dB)	Digital Gain Steps (dB)	OIP3 (dBm)	OIP2 (dBm)	OP_{1dB} (dBm)	HD2 (dBc)	HD3 (dBc)	NF (dB)
MAX2065	Analog/digital	50 to 1000	-43 to +19	1	41.5	60	18.5	-63	-80	6.6
MAX2066*	Digital	50 to 1000	-11 to +20	1	42	60.5	18.5	-63	-80	5.5
MAX2067*	Analog	50 to 1000	-9.5 to +21.5	—	42	61	18.5	-63	-80	4.2

SPI is a trademark of Motorola, Inc.
WiMAX is a trademark of the WiMAX Forum.
*Future product—contact factory for availability.

Technical Support
www.maxim-ic.com/support

MAXIM DIRECT
www.maxim-ic.com/shop

AVNET electronics marketing
www.avnet.com

MAXIM
www.maxim-ic.com/program-vga

For a free sample, visit www.maxim-ic.com/samples or call 1-800-998-8800

inverters, and a parallel electrical connection between the flip-flops' outputs replaces the OR gates. EDN

REFERENCES

1 "Using Wire-OR Ties In ECLinPS Designs," Application Note AN1650/D, On Semiconductor, www.onsemi.com/pub/Collateral/AN1650-D.PDF.

2 "Dual D Type Master Slave Flip-Flop," MC10H131 Data Sheet, On Semiconductor, www.onsemi.com/pub/Collateral/MC10H131-D.PDF.

3 "Triple 2-Input Exclusive OR/Exclusive NOR Gate," MC10H107 Data Sheet, On Semiconductor, www.onsemi.com/pub/Collateral/MC10H107-D.PDF.

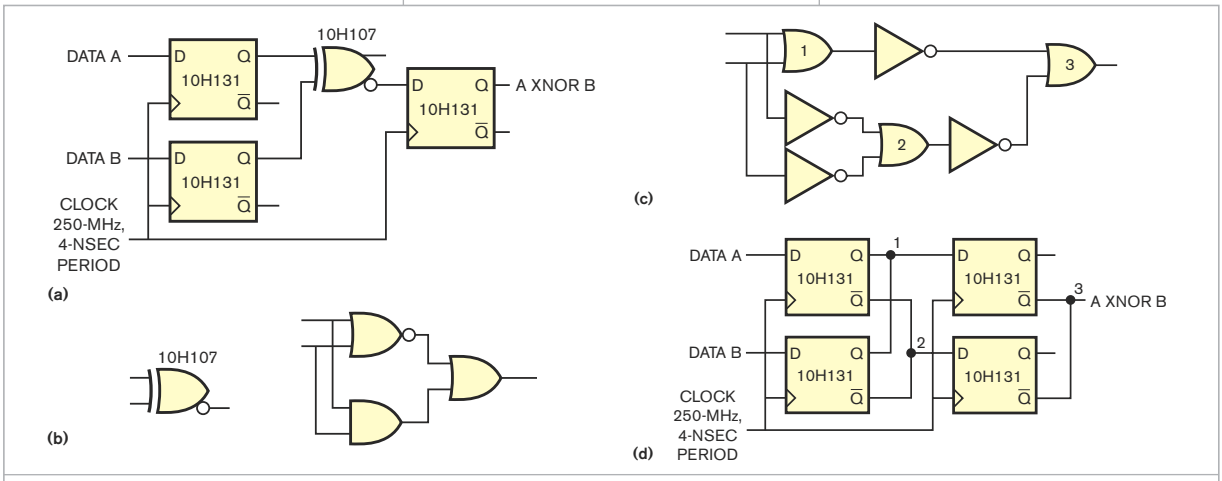


Figure 1 The XNOR comparison of inputs A and B results in too much propagation delay to guarantee setup at the final flip-flop's input (a). The equivalent XNOR circuit uses NOR, AND, and OR gates (b), and OR gates and inverters realize the XNOR function (c). You can also implement the circuit using wired ORs (d) to eliminate the interflop XNOR-gate delay and almost double the usable clocking speed.

LINEAR TECHNOLOGY

DESIGN NOTES

Compact Triple Step-Down Regulator Offers LDO Driver and Output Tracking and Sequencing – Design Note 441

Tiger Zhou

Introduction

Typical industrial and automotive applications require multiple high current, low voltage power supplies to drive everything from disk drives to microprocessors. The LT®3507 triple step-down converter fits easily into these applications. It is simple and compact compared to multi-chip solutions.

The LT3507 is a single IC current mode triple step-down regulator with internal power switches and a low dropout linear regulator driver. The switching converters are capable of generating one 2.4A output and two 1.5A outputs. All three converters are synchronized to a single oscillator, with the 2.4A output running antiphase to the other two converters, thereby reducing input ripple current. Each converter has independent shutdown and soft-start circuits and generates a power good signal when its output is in regulation, simplifying both supply sequencing and the interface with microcontrollers and DSPs. Separate input pins for each regulator offer additional flexibility; regulators can be cascaded to reduce circuit size, or each regulator can draw power from a different input source.

The switching frequency is set with a single resistor between 250kHz to 2.5MHz. High switching frequency allows the use of small inductors and capacitors resulting in a very compact triple output supply. The constant switching frequency, combined with low impedance ceramic capacitors, results in low output ripple. With its wide input voltage range of 4V to 36V, the LT3507 regulates a broad array of power sources including 5V logic rails, unregulated wall transformers, lead acid batteries and distributed power supplies.

6V to 36V Input to Four Outputs—1.8V, 3.3V, 5V and 2.5V—One IC

The triple converter accommodates a 6V to 36V input voltage range and is capable of supplying up to 2.4A, 1.5A and 1.5A, respectively. The 20mA LDO driver output can drive an NPN transistor to provide a fourth low noise rail. Figure 1 shows a typical application for four outputs—1.8V at 2.4A, 3.3V at 1.3A, 5.0V at 1.5A and 2.5V at 0.2A—from a 6V-36V input supply.

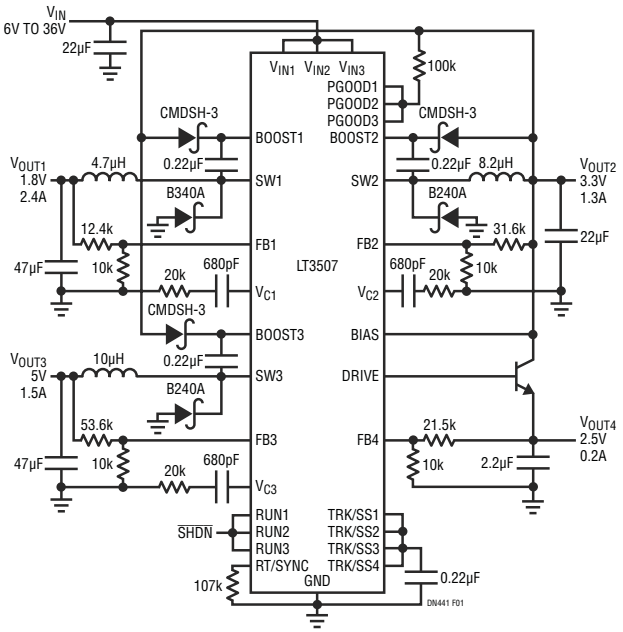


Figure 1. A 4-Output Supply Including a Low Noise LDO

Low Ripple High Frequency Operation Even at High V_{IN}/V_{OUT} Ratios

High frequency operation minimizes solution size, but one obstacle to high voltage (36V), high frequency (MHz) operation of monolithic step-down regulators is the minimum on-time constraint. Due to an internal logic propagation delay, a step-down regulator must remain on for a minimum time interval for proper operation. Otherwise, the converter operates in pulse-skipping mode at high input-to-output ratios, which has the undesirable side effect of increasing output ripple. For example, the application in Figure 1 best operates at 450kHz when the input is 36V and the output is 1.8V.

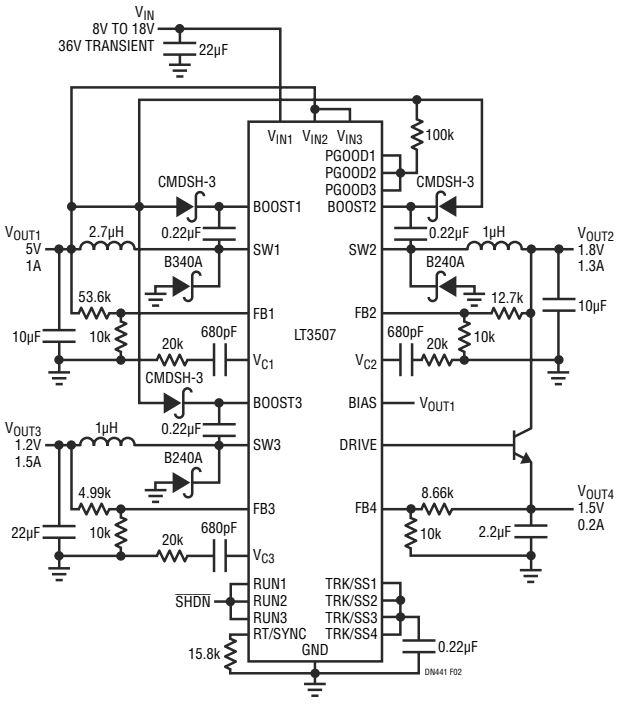


Figure 2. Cascading Supplies Maintain High Frequency Operation Even with High V_{IN}/V_{OUT} Ratios

However, the LT3507 has a built-in solution to this problem. By cascading the first converter and the other two, as shown in Figure 2, all three converters can be operated at 2MHz without pulse-skipping mode.

Input Voltage Lockout and Sequencing

The LT3507's under- and overvoltage lockouts can be programmed with external resistors. When the schematic in Figure 2 is modified as in Figure 3, the LT3507 will accept V_{IN} up to 36V but operate only when V_{IN} is between 8V to 18V. This prevents the IC from operating during unintended or fault conditions, allowing the circuit designer to reduce the size of the external components. Figure 3 also shows a simple sequencing scheme: channel 1's power good indicator is tied to the tracking pins of the other three channels. Figure 4 shows the resulting start-up sequence, with channel 1 starting first and the remaining channels tracking during their start-up. Other sequencing and tracking examples can be found in the data sheet.

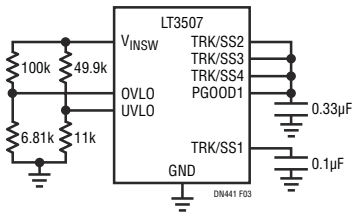


Figure 3. External Resistors Program the Input Voltage Lockout; PGOOD1 Determines Sequencing and Tracking

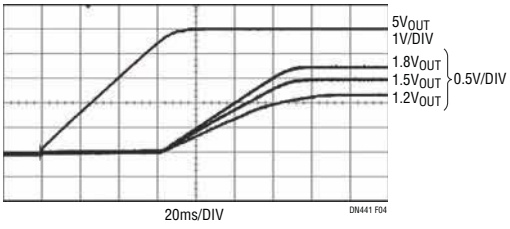


Figure 4. Channel 1 Starts First, the Others Follow and Track

An additional feature of LT3507 is the low noise LDO output. Figure 5 shows the LDO output ripple is reduced from the preregulated Channel 2 output.

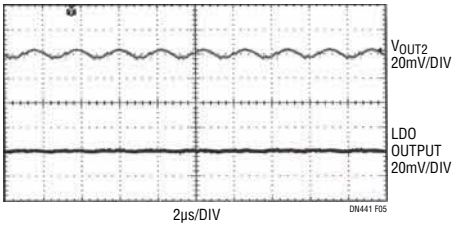


Figure 5. Low Noise LDO Output: Top Trace is Channel 2 Output, Bottom Trace is Channel 4 LDO Output

Conclusion

The LT3507 integrates three buck regulators and an LDO driver in a QFN (5mm × 7mm) package, offering a compact solution for multiple-rail systems. Separate inputs for each converter offer wide design freedom, while separate PG indicators and TRK/SS pins further extend tracking and sequencing flexibility.

Data Sheet Download

www.linear.com

For applications help,
call (408) 432-1900, Ext. 3223

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn441f LT/TP 0508 392K • PRINTED IN THE USA

Small things make a big difference.

Melexis' Award-Winning Triaxis™ Hall-Effect ICs Simplify 360° Rotary Position and Joystick Applications

Small Things

At 4mm X 5mm, the MLX90316 and MLX90333 are Award-winning Hall-effect position sensor ICs which were designed specifically for 360 degree rotary position and contactless joystick applications. Both the MLX90316 and the MLX90333 belong to the Triaxis™ family of Hall-effect ICs, which employs patented IMC (Integrated Magnetic Concentrator) technology and standard Mixed Signal CMOS IC fabrication to achieve its outstanding performance.

Triaxis™

The Big Difference

Melexis' Triaxis™ technology senses the position of a common magnet within a 15mm proximity of the chip. This allows accurate and repeatable 3-Dimensional position sensing without the need for exotic magnetic circuits or constant mechanical and electronic calibration.

The MLX90316 and MLX90333 solve the sensing and signal problems so designers can concentrate on making the best rotary controls and joysticks.

Small things make a big difference.

For more information call us at
1 (603) 223 2362
or visit our website:
www.melexis.com

Melexis
Microelectronic Integrated Systems

Support **Across The Board**™

Bryan Fletcher
Avnet
Global Technical Marketing
Manager

David Loftus
Xilinx
Vice President / General Manager
General Products Division (GPD)

Bringing Products to Life.

At Avnet Electronics Marketing, support across the board is much more than a tagline for us. From design to delivery – we are deeply committed to driving maximum efficiency throughout the product lifecycle.

The Challenge
When the world's largest FPGA maker Xilinx was mounting the launch of its latest Spartan™-3 Generation family of low-cost FPGAs, the company wanted to ensure designers would have everything they need to compete in the highly competitive high-volume market. Xilinx turned to longtime partner Avnet to lend its technical expertise in creating a complete solution.

The Solution
Avnet spent countless engineering hours alongside Xilinx – developing a comprehensive solution of starter kits, development boards, and Speedway™ educational workshops. With Xilinx® Spartan-3 Generation FPGAs and Avnet's support across the board, designers have access to all they need to save up to 50 percent in total system cost over competing FPGAs.

Visit **www.em.avnet.com/xilinxspartan3kits** to learn more about Spartan-3 solutions and to purchase a **Spartan-3A evaluation kit for only $39!**

XILINX®

AVNET® electronics marketing

Accelerating Your Success™

Avnet Green Initiative

Supplier Authorized Distributor

1 800 332 8638
www.em.avnet.com

productroundup

SENSORS AND TRANSDUCERS

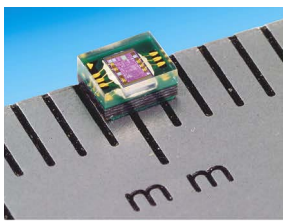
Programmable meter includes integrated diagnostics

Targeting use in analog sensors and transducers, the TDRO-10 programmable meter integrates diagnostics for input and output. Features include two-button English-language programming with a 67-msec update rate and a six-digit LED display with half-inch numbers and a 6-msec refresh rate. Measuring 3.78×1.89×1 in., the meter allows 0 to 10V standard-sensor inputs or 4 to 20 mA with overvoltage protection. One version provides a 16-bit analog output and two or four programmable PNP digital outputs with 100% scalable analog retransmission; another version is read-only with no digital output. The TDRO-10 programmable meter costs $100.

Transducers Direct, www.transducersdirect.com

Single-chip proximity and ambient-light sensor integrates optical filters and photo diodes

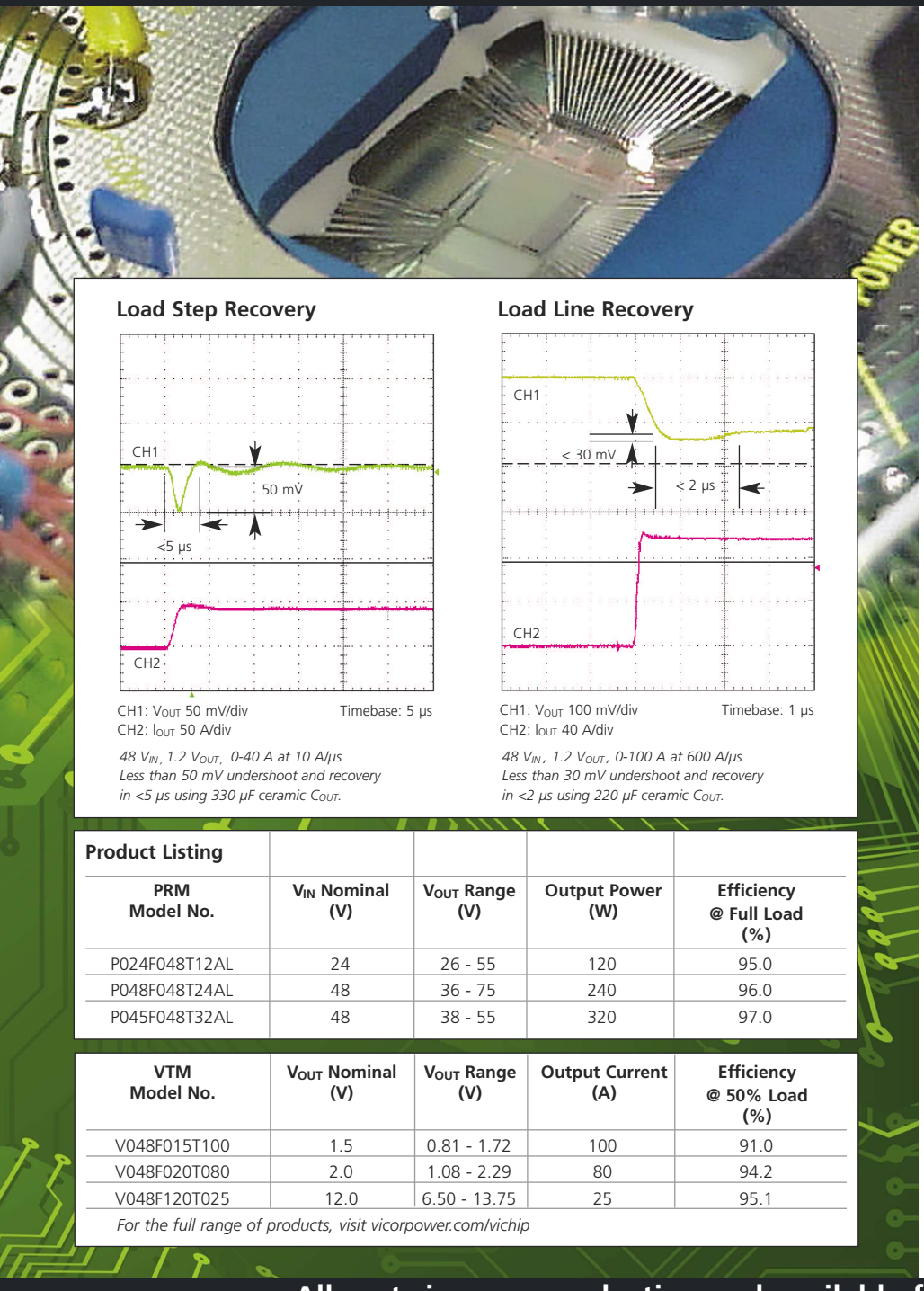
The vendor's Filtron technology allows the single-chip CM3612 infrared-proximity and ambient-light sensor to mimic the brightness sensor of the human eye by detecting wavelengths in the 450- to 650-nm range. The chip features a digital lowpass filter for removing fluorescent-light flicker, a 12-bit ADC, a DSP, a temperature-compensation circuit, an



All the Speed
None of the Bulk

Visit us at PCIM Booth 12-431

V•I Chip power components provide fast response and maintain power integrity



Load Step Recovery

CH1: V_{OUT} 50 mV/div Timebase: 5 µs
CH2: I_{OUT} 50 A/div

48 V_{IN}, 1.2 V_{OUT}, 0-40 A at 10 A/µs
Less than 50 mV undershoot and recovery
in <5 µs using 330 µF ceramic C_{OUT}.

Load Line Recovery

CH1: V_{OUT} 100 mV/div Timebase: 1 µs
CH2: I_{OUT} 40 A/div

48 V_{IN}, 1.2 V_{OUT}, 0-100 A at 600 A/µs
Less than 30 mV undershoot and recovery
in <2 µs using 220 µF ceramic C_{OUT}.

Product Listing

PRM Model No.	V_{IN} Nominal (V)	V_{OUT} Range (V)	Output Power (W)	Efficiency @ Full Load (%)
P024F048T12AL	24	26 - 55	120	95.0
P048F048T24AL	48	36 - 75	240	96.0
P045F048T32AL	48	38 - 55	320	97.0

VTM Model No.	V_{OUT} Nominal (V)	V_{OUT} Range (V)	Output Current (A)	Efficiency @ 50% Load (%)
V048F015T100	1.5	0.81 - 1.72	100	91.0
V048F020T080	2.0	1.08 - 2.29	80	94.2
V048F120T025	12.0	6.50 - 13.75	25	95.1

For the full range of products, visit vicorpower.com/vichip

32.5 x 22.0 x 6.6 mm
1.28 x 0.87 x 0.26 in

RoHS

V•I CHIP
FACTORIZED POWER

- **Maximizes processor speed**
- **Simplifies power management software**
- **Eliminates processor faults**
- **No bulk electrolytic capacitors**
- **Minimal footprint**

The MHz PRM regulator and the low AC impedance (less than 1 mΩ) VTM transformer deliver the fastest transient response without bulk capacitance at the load. V•I Chips enable flexible load line and compensation techniques which allow for matching of power source to the load.

Call 800-735-6200
for design support.
Order evaluation boards
now at vicorpower.com/vichip

All parts in mass production and available from stock

800-735-6200 **vicorpower.com/fpaedn1** VICOR

productroundup

SENSORS AND TRANSDUCERS

oscillator, and an infrared-emitter driver. The sensor has a 2.6 to 3.7V operating voltage and a 130-mA typical current consumption. The device extends battery life using a proximity function, enabling portable products to automatically turn off screens, and an ambient-light sensor allows for automatic adjustment of screen brightness to match external-light conditions. The proximity sensor can deactivate a touchscreen, preventing dialing when in contact with a user's hand. Using an I^2C interface, the sensor allows the ambient-light value to be read from a 12-bit register; the CM3601 version uses a DAC instead of the I^2C interface to output the ambient-light value as an analog-output signal. Both devices use an optical bandpass filter, allowing only the 450- to 650-nm green-light band to a photo diode. Available in an OPLGA package measuring 2.35×1.8×1 mm, the CM3601 and CM3612 cost $1.20 and $1.50, respectively.

Capella Microsystems, www.capella micro.com

Hall-effect sensors have user-adjustable bandwidth

A user-adjustable bandwidth suits these low-noise, linear-Hall-effect sensors for high-current sensing. The A1360, A1361, and A1362 provide 0.7- to 1.4-mV/G, 1.5- to 4.5-mV/G, and 4.5- to 16-mV/G programmable sensitivity ranges, respectively. Features include 8-mV noise, a 0%/°C flat-temperature coefficient, a −40 to +150°C temperature range, and a 50-kHz typical bandwidth. The A136x has a capacitor to ground on the filter pin, allowing tuning of the device bandwidth from 50 kHz to less than 100 Hz. The sensors provide a voltage output proportional to the applied magnetic field. The quiescent output voltage is user-adjustable to 50% bidirectional or 10% unidirectional of the supply voltage. Available in the vendor's 1-mm, lead SIP-4 KT package, the A1360, A1361, and A1362 cost $1.28 (1000) each.

Allegro MicroSystems, www.allegromicro.com

IP-based platform has WSN architecture

Targeting energy management, compliance and safety enforcement, environmental monitoring, and energy-generation technologies, the PhyNet IP (Internet Protocol)-based platform uses a WSN (wireless-sensor network) architecture and requires no co-location of individual sensor networks, with the server-based functions controlling the devices. Individual sensor nodes communicate directly with the IP devices on the enterprise network, regardless of the connection medium. The platform's architecture includes a PhyNet server, a PhyNet router, and the vendor's nodes. An entry-level system costs $7995 and includes a PhyNet server, two PhyNet routers, 10 analog IPsensor nodes, and two IPserial nodes. The product is scalable by adding individual components.

Arch Rock Corp, www.archrock.com

GEM thermistor provides stability over time

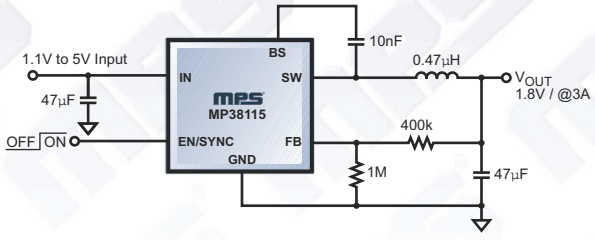
The 55000 Series GEM (glass-encapsulated-material) thermistor has an automated assembly. The device provides a 0.012°C shift at 100°C after 10 months and a 2252Ω to 30-kΩ resistance range at 25°C. Features include ±0.1°C interchangeability over a 0 to 70° temperature range, −80 to +200°C operating-temperature range, and a hermetically sealed package. Available as 0.1C or 0.2C parts, the devices cost $8.40 and $6, respectively.

Measurement Specialties, www.meas-spec.com

LDO's Burning You Up?
Low Voltage 4A Synchronous Switching Regulator Operates Down to 1.1VIN

Reduce Power Loss Up to 65%!

Cooler
Sync. Step-Down Switcher



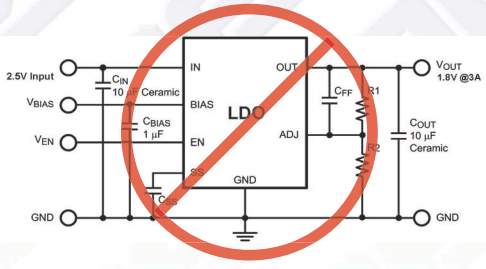
Actual Size QFN10 ($9mm^2$)

2.5V Input to 1.8V Output @ 3A

Pdiss = 0.74W!

VS

LDO
No Longer Recommended for New Designs



Actual Size SOIC8 ($30mm^2$)

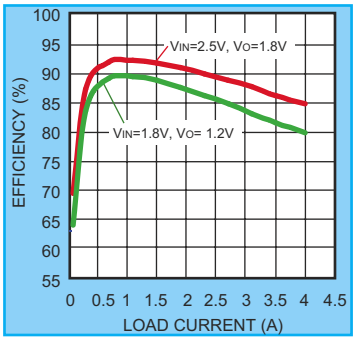
2.5V Input to 1.8V Output @ 3A

Pdiss= 2.1W!

MP38115 Features:

- *4A Load Current*
- *Input Supply Range: 1.1V-5V*
- *All Ceramic Output Capacitors Design*
- *1.5MHz Fixed Switching Frequency*
- *Ultra Small Footprint: $9mm^2$ QFN*

MP38115 Efficiency vs Load Current



Highest Efficiency Sync Step-Down Switching Regulators

Part	VIN (V)	IOUT (A)	Switch Frequency	Freq Sync IN	Package
MP38115	1.5 - 5.0	4	1.5MHz	NO	QFN10 (3x3)
MP2207	3.0 - 16	4	1.3MHz	NO	QFN10 (3x3)
MP38871	4.5 - 25	10	600kHz	Up to 1MHz	QFN10 (3x4)

DC to DC Converters CCFL / LED Drivers Class D Audio Amplifiers Linear ICs

ISO9001:2001 Certified

LEAD FREE RoHS COMPLIANT

Monolithic Power Systems®
The Future of Analog IC Technology®
www.monolithicpower.com

AVNET Memec

productroundup

MICROPROCESSORS

FPGA family has low power consumption

The 120-I/O AGLP030 Igloo Plus low-power FPGA consumes 5 µW in a design requiring 100 I/Os. The FPGA supports independent Schmitt-trigger inputs, hot swapping, and flash-freeze bus hold. The family comes in three 1.2V devices that have 30,000 to 125,000 gates. Available in a CS201 package, the 120-I/O AGLP030 costs $1.95.

Actel Corp, www.actel.com

ARM9 microcontroller family provides Ethernet and On-The-Go USB

Based on the ARM926EJ processor, the 32-bit LPC3200 ARM9 microcontroller family combines the processor core with a vector floating point, an LCD controller, an Ethernet MAC (media-access controller), and a bus matrix. Features include an I^2C, an I^2S, an SPI (serial-peripheral interface), UARTs, On-The-Go USB, and PWMs (pulse-width modulators). Additional features include a 10/100 Ethernet MAC and a 24-bit LCD controller supporting STN (supertwist-nematic) and TFT (thin-film-transistor) panels. Suiting DDR, SDR, SRAM, and flash-memory devices, the family provides the option of booting up from NAND flash, SPI memory, UART, or SRAM. Prices for the LPC3220, LPC3230, LPC3240, and LPC3250 devices range from $6.95 to $8.25 (10,000).

NXP Semiconductors, www.nxp.com

Development environment allows writing of low-level Java code

The Perc Pico development environment for Wind River's VxWorks real-time operating system and the Wind River workbench development suite allows developers to write low-level Java code for device drivers and interrupt handlers, telecommunications-control planes, and signal processors for multimedia. The environment offers a memory footprint measuring in the hundreds of kilobytes. Available for VxWorks targeting the PowerPC architecture, as well as Windows and Linux/x86 platforms, the device is portable to most processor architectures for real-time operating systems and bare-board platforms. Prices for the Perc Pico development tools start at $25,000 for an unlimited number of developers.

Aonix, www.aonix.com

Processor companion has an integrated 32-kHz watch crystal

The FM3135 3V processor companion combines a 64-Kbit FRAM and an enhanced RTC (real-time clock) with an alarm and programmable-frequency clock output and an integrated 32-kHz watch crystal. The processor companion uses a two-wire bus for accessing the memory and controlling the RTC. The device has a 2.7 to 3.6V operating voltage over the −40 to +85°C temperature range. Available in a SOIC-20 package, the FM3135 processor companion costs $3.20 (10,000).

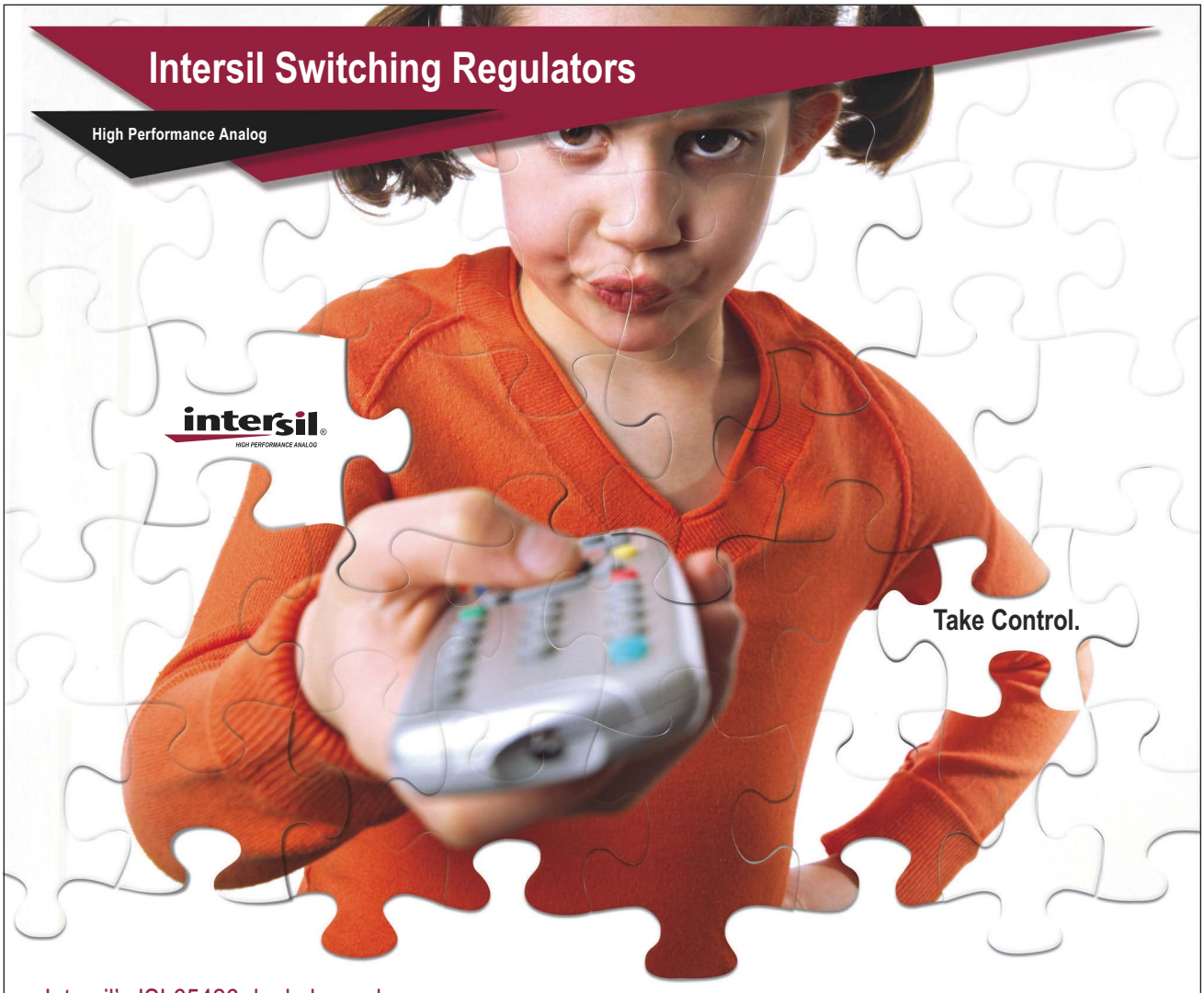
Ramtron International Corp, www.ramtron.com

High-end debugger functions over JTAG and Nexus

Targeting AVR and AVR32 microcontrollers, the AVR One high-end on-chip debugger uses AVR32 devices' four-pin JTAG port, Nexus port, and 8-bit parallel port. The debugger monitors and modifies system be-

Intersil Switching Regulators

High Performance Analog



Intersil's ISL65426 dual-channel, synchronous buck regulator has **user-configurable power blocks that enable quick design and reconfiguration of power supply systems** for FPGAs, CPLDs, core processors, and ASICs.

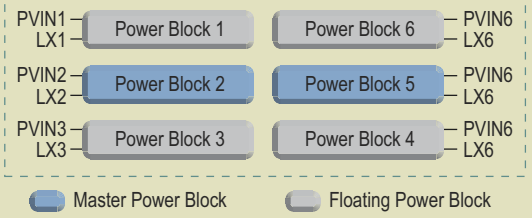
ISL65426 Key Features:

- 180° out-of-phase operation
- Startup in a pre-biased load
- Independent output soft-start
- Stable all ceramic solutions
- High efficiency: 95%
- ±1% system accuracy over temperature

Output Current Configurations

I_{1SET}	I_{2SET}	I_{OUT1}	Channel 1 Connections	I_{OUT2}	Channel 2 Connections
1	1	3A	LX1, LX2, LX3	3A	LX4, LX5, LX6
1	0	4A	LX1, LX2, LX3, LX4	2A	LX5, LX6
0	1	5A	LX1, LX2, LX3, LX4, LX6	1A	LX5
0	0	2A	LX1, LX2, LX3, LX4, LX6	4A	LX3, LX4, LX5, LX6
Invalid LX Configurations: SS Prevented					
X	X	1A	LX2	5A	LX1, LX3, LX4, LX5, LX6

Six Integrated 1A Power Blocks



Go to **www.intersil.com** for samples, datasheets and support

Intersil – Switching Regulators for precise power delivery.

intersil®
HIGH PERFORMANCE ANALOG

productroundup

MICROPROCESSORS

havior throughout the microcontroller without interrupting or affecting the timing of the program running on the microcontroller. The debugger captures real-time-trace data and reconstructs the steps the processor takes using a 2-Gbyte data buffer. The AVR322 Studio project manager and debugger front-end Version 2 supports the AVR One. The AVR One costs $599.

Atmel Corp, www.atmel.com

16-bit microcontrollers integrate a capacitive-touch peripheral

Adding to the vendor's 16-bit PIC-24F microcontroller family, the nine devices in the PIC24FJ256GA1 product line provide a 2.6-mA standby current, 256-kbyte flash memory, and 16-kbyte RAM. The royalty-free Touch Sensing Solution software-development kit and the CTMU (charge-time-measurement-unit) peripheral allow designers to add a capacitive-touch user interface requiring no external components. Peripherals include four UARTs, three SPIs (serial-peripheral interfaces), and three I^2C ports. Additional features include 23 independent timers and the peripheral-pin-select pin-mapping function. Available in TQFP-64, -80, and -100 packages and in commercial- and extended-temperature ranges, the PIC-24FJ256GA1 microcontroller family costs $3.39 (10,000). Owners of the Explorer 16 development board can buy a $25 plug-in module.

Microchip Technology, www.microchip.com

COMPUTERS AND PERIPHERALS

1000W power supply aims at gaming systems

The HX1000W power-supply unit claims a 1000W output at 50°C. Suiting multicore processors and graphics-processing systems, the supply provides an independent dual-12-rail design and a 140-mm temperature-controlled fan. Also known as the CMPSU-1000W, the HX1000W power-supply unit costs $279.99.

Corsair, www.corsair.com

Five 17- and 19-in. LCDs claim an improved brightness

Replacing the vendor's AccuSync 2 Series LCD family, the AccuSync 3 Series product family includes the 17-in. ASLCD73VX, ASLCD73-VX-BK, and the multimedia ASLCD73-VXM-BK displays, as well as the 19-in. ASLCD93VX-BK and the multimedia ASLCD73VXM-BK displays. The displays have 700-to-1 and 800-to-1 contrast ratios for the 17- and 19-in. models, respectively. Features include 300-cd/m^2 brightness, 1280×1024-pixel native-resolution, 5-msec Rapid-Response technology, and dual-input technology. The multimedia displays also feature built-in speakers. The 17-in. ASLCD73VX and ASLCD73VX-BK cost $224.99, and the ASLCD73VXM-BK costs $239.99. The 19-in. ASLCD93VX-BK and ASLCD-93VXM-BK cost $254.99 and $274.99, respectively.

NEC Display Solutions, www.necdisplay.com

Universal adapter aims at 2.5- or 3.5-in. IDE or SATA hard drives

The DriveWire universal hard-drive adapter provides a USB

productroundup

COMPUTERS AND PERIPHERALS

connection to 2.5- or 3.5-in. IDE (integrated-drive-electronics) or SATA (serial-advanced-technology-attachment) drives. The adapter comes with the vendor's upgrade suite, featuring EZ Gig II cloning and imaging software for Windows and Shirt Pocket's SuperDuper For Macs. Features include three hard-drive connections, a SATA connector, a 44-pin connector for 2.5-in. notebook IDE/PATA (parallel-ATA) drives, and a 40-pin connector for 3.5-in. desktop IDE/PATA hard drives. The DriveWire adapter costs $39.99 and has a one-year limited warranty.

Apricorn, www.apricorn.com

Graphics card has 512 Mbytes of GDDR3 frame-buffer memory

The Verto GeForce 9600 GT graphics card features a 512-Mbyte GDDR3 frame-buffer memory and a 650-MHz core clock. Supporting Microsoft's DirectX 10 shader model 4.0, the card also provides a 57.6-Gbps memory bandwidth and a texture-fill rate of 20.8 billion/sec. The device suits PCIe (PCI Express)-bus architecture and supports NVideo SLI technology. The Verto GeForce 9600 GT graphics card costs $199.99.

PNY Technologies, www.pny.com

PC chassis provides three cold-air intakes

With an aluminum construction, a piano-black finish, and an integrated handle, the GT3 PC chassis supports full-sized ATX (advanced-technology-extended) motherboards and full-height, double-slot graphics cards. The device provides three cold-air intakes for the processor and memory, add-in cards, and power supply. The 370W ATX 2.01 power supply is certified for all GT3 configurations. The GT3 PC chassis costs $99.

GTR Tech Corp, www.gtrtechcorp.com

ExpressCard replaces reader-only version

The 21-in-1 multimedia-memory-card Reader and Writer aims at Express Card/34 and ExpressCard/54 slots. The device replaces the vendor's reader-only version at the same price. The ExpressCard/34 costs $29.95.

Sonnet Technology, www.sonnettech.com

Desktop board allows for eight-core processing

Supporting multicard-graphics devices from ATI and Nvidia, the dual-socket QX9775 Core 2 Extreme processor supports two quad-core processors, providing an eight-core platform. Each processor provides 12 Mbytes of L2 cache, a 1600-MHz system bus, and four 3.2-GHz cores. The QX9775 Core 2 Extreme costs $1499, and the vendor's D5400XS desktop board costs $649.

Intel Corp, www.intel.com

RAID-controller family provides as many as 28 ports

Using the Intel IOP348 I/O processor, the vendor's Series 5 family improves its RAID (redundant-array-of-inexpensive-disks)-controller technology by providing connectivity for as many as 28 internal and external ports. The Intel IOP348 processor delivers a 1.2-GHz core speed. The device includes four- and eight-internal-port devices and an eight-external-port device. The family also includes eight-, 16-, 20-, and 28-port devices with four external ports and four, 12, 16, and 24 internal ports. Prices for the RAID controllers range from $425 to $1595, depending on the number of ports.

Adaptec, www.adaptec.com

EDN ADVERTISER INDEX

Company	Page
Actel Corp	6
Agilent Technologies	29, 39
Analog Devices Inc	23, 25
	16-A-H
Ansoft Corp	48
austriamicrosystems AG	72
Avnet Electronics Marketing	76
Bias Power LLC	85
Bokers Inc	85
Bourns Inc	3
Coilcraft	13
CUI Inc	60
Cypress Semiconductor	C-4
Design Automation Conference	16
Digi-Key Corp	1
EMA Design Automation	45
Express PCB	62
Freescale Semiconductor	31
Infineon Technologies AG	52
Intersil	35
	54, 82
Jameco Electronics	2
Keil Software	84
Lambda Americas	61
LeCroy Corp	C-2
Linear Technology Corp	63
	64, 67
	73, 74

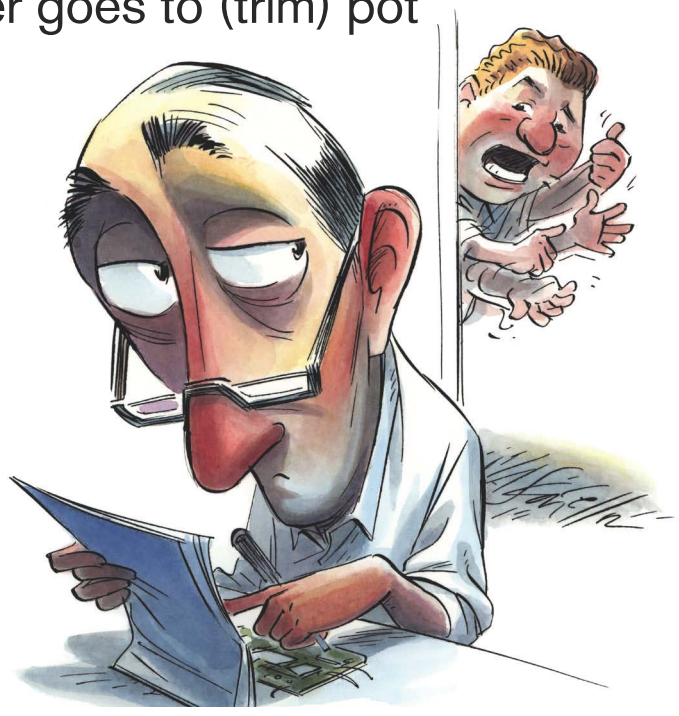
Company	Page
Maxim Integrated Products	69, 71
Melexis Inc	75
Mentor Graphics	79
	81, 83
Micrel Semiconductor	14
Microsoft Corp	10,11
Monolithic Power Systems	80
Mouser Electronics	8
National Instruments	4, 15
NewarkInOne	27
Numonyx	C-3
Panasonic Electric Works	77
Pico Electronics	36, 46
Rabbit Semiconductor	38
Samtec USA	59
Simlab Software GmbH	47
Tern	85
Texas Instruments	19, 21
	37, 43
	32-A-B
That Corp	62
Toshiba America	32
Vicor	53, 78
Vision Components	51

EDN provides this index as an additional service. The publisher assumes no liability for errors or omissions.

EDN product mart

This advertising is for new and current products.

Laser goes to (trim) pot



We had finished final tests on a transponder whose function was to take in a SONET (synchronous-optical-network) data stream at a 1310-nm wavelength and retransmit the data at 1550 nm for use in bidirectional coarse-wave-length-division multiplexing on a single optical fiber. The product had to withstand outdoor environmental ambient-temperature variations of −40 to +65°C and did not have the power budget to allow laser heating or cooling to a constant temperature. We installed various 1550-nm-laser types on the basic PCB (printed-circuit board) for the power and distance options. When cold, a laser requires small current drive. When hot, the laser requires the current drive to rise to maintain lasing threshold and sufficient modulation depth. Turning the laser completely off during modulation minimums would cause a start-up delay that would shorten the next pulse width. Thus, we had to keep the laser alive at all times with at least 10 dB between minimum threshold and maximum pulse-power levels.

We used a self-training technique that placed one-board-fits-all production units with their various laser types into an environmental chamber, where we ramped the temperature from −40 to +65°C. During training, the control processor used analog-to-digital conversion and EEPROM data storage to record the individual laser's temperature-dependent drive requirements at all operational temperatures.

A feedback loop from the laser's rear-facet photodiode controlled the laser's average power as set by a mechanical trim pot and followed temperature variations to maintain constant average optical power. The ADC and processor monitored this average current as an indirect temperature measurement; the processor also used a DAC to search for the required laser current for a 10-dB power increase at each temperature. The resulting training data was stored in an EEPROM and retrieved during normal operation, again using the ADC and DAC functions.

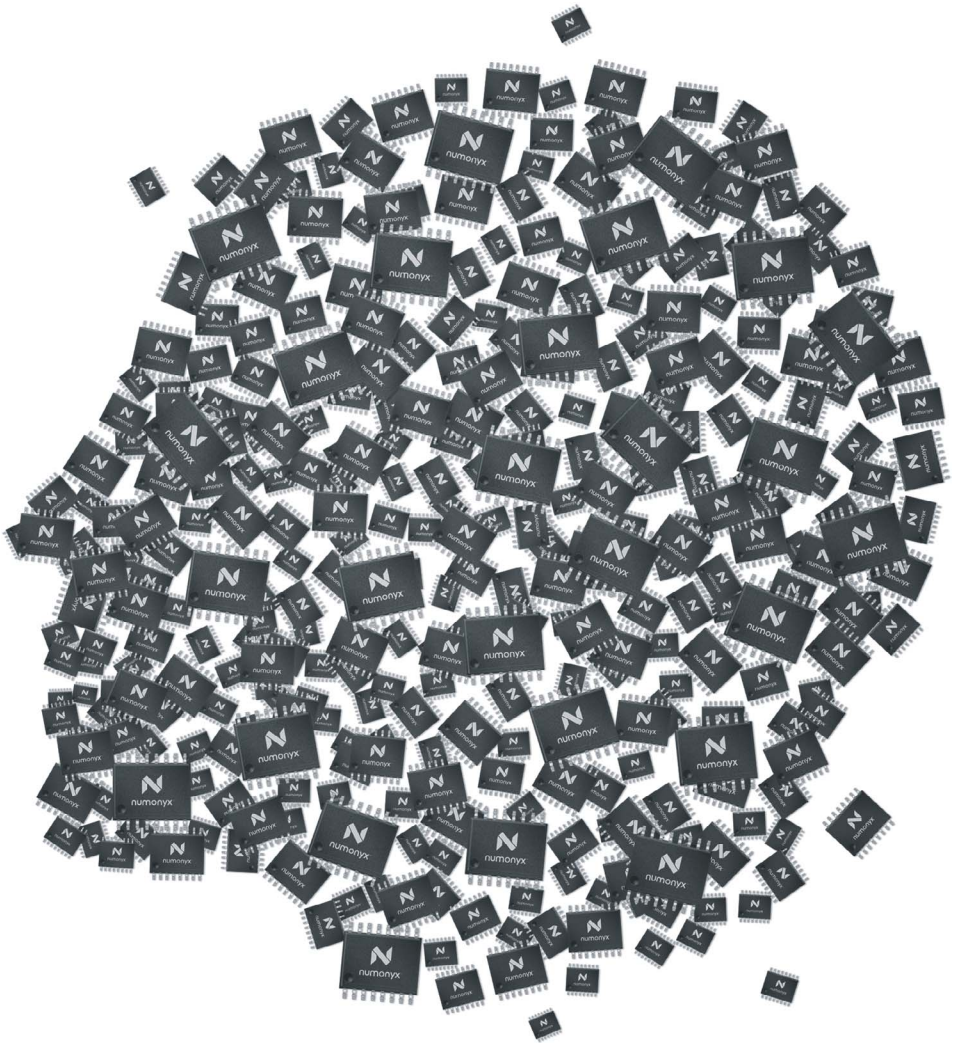
During the initial lab tests of a 1-mW laser, I noticed that the trim-pot setting was close to the end of its range, and the resulting coarse mechanical response was difficult to adjust. I changed the trim pot from the 10 kΩ for the low-power lasers to 1 kΩ for the high-power laser. This change placed the trim-pot wiper close to the center of its range for easier adjustment.

A customer later wanted a sample of the high-power, long-reach version, so our production technician took a pretested, low-power unit from stock, swapped out the laser, and tweaked the trim pot for 0 dBm, as required. He did not swap out the original 10-kΩ trim pot. During the training-temperature ramp, all looked good until the temperature reached about −5°C. Then, the laser power became erratic, and we had to quickly find and fix the problem. We first replaced the laser to no avail. In the third trial temperature ramp, the laser power had not yet started bouncing up and down when I suddenly remembered the 10-kΩ trim pot and its coarse-setting difficulty. Sure enough, the trim pot was still the 10-kΩ value set close to the end of its range and in this position was mechanically sensitive to temperature variations. I changed the trim pot to 1 kΩ, retweaked for 0 dBm near the thermally benign wiper center, and restarted the training-temperature ramp. This time, there were no erratic power fluctuations, and the recorded modulation level data was nicely monotonic.

The incident resulted in a procedure for better written communication. A "traveler" sheet containing the unit's history already accompanied each production unit. All we had to do was place a note on the sheet stating that, if you replaced the standard laser with a high-power one, you needed to change the trim pot, too. EDN

You can reach design consultant Glen Chenier at glen@teetertottertreestuff.com. Share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

DANIEL VASCONCELLOS

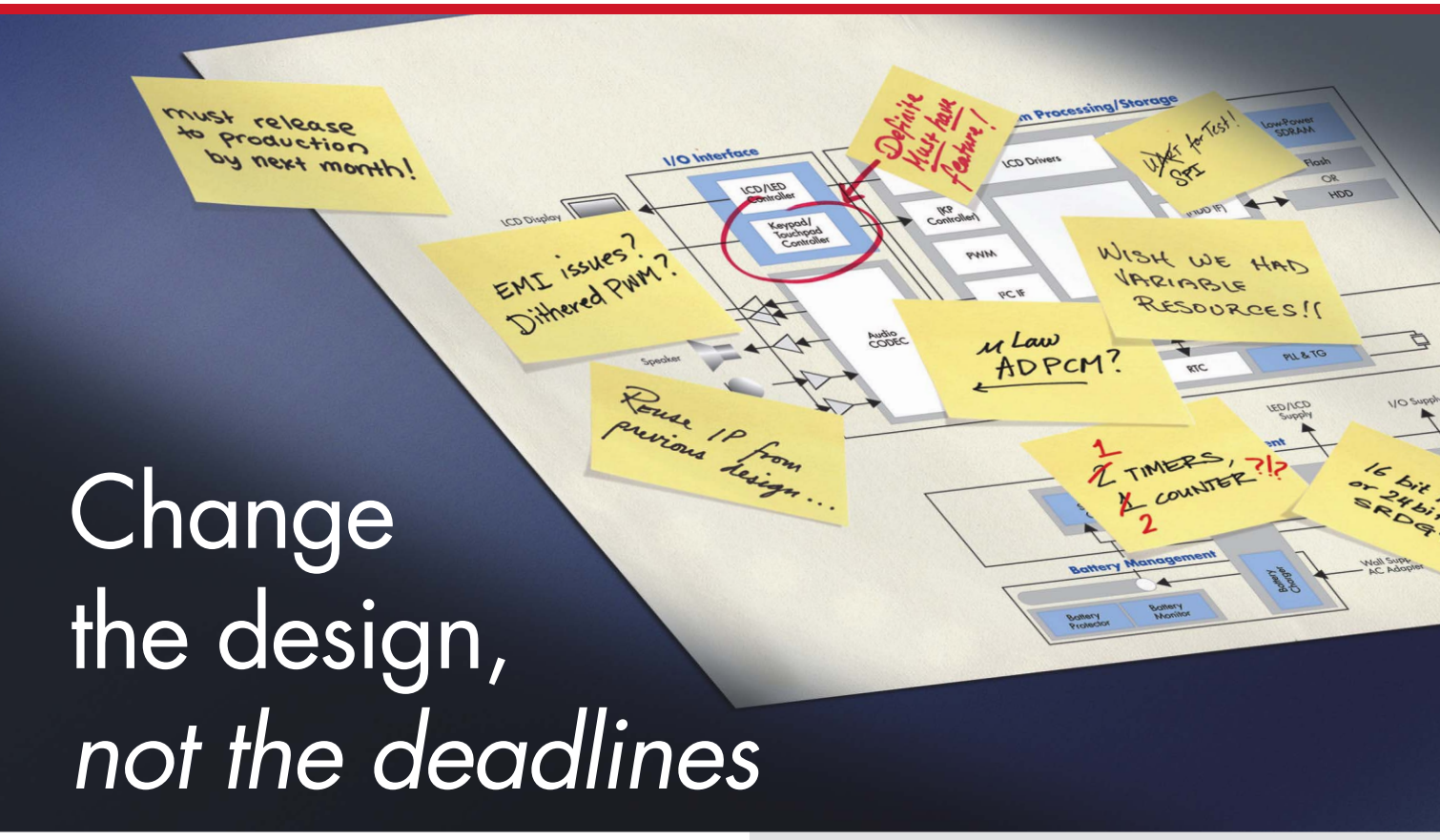


We're changing the face of memory.

Meet Numonyx.™ A new company with a single focus—creating advanced memory solutions. Built on the people and heritage of STMicroelectronics* and Intel*, we deliver a complete range of products including NOR, NAND, MCP including RAM, and PCM. By working closely with customers to develop innovative memory technologies and services, our goal is to do more than just help you bring products to market faster. It's to create a new experience in memory.

numonyx.com

numonyx™



Change the design, *not the deadlines*

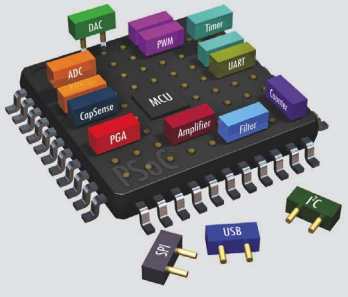
PSoC flexibility enables changes anytime: at concept, through production, in the field. Specifications change constantly. Yet pressures to differentiate, minimize costs, and speed time-to-market remain the same. To stay ahead of the curve, you need flexibility, programmability, and scalability. PSoC's unique programmable architecture delivers this and more. Futureproof your design; make PSoC your agent of change.

PSoC delivers:

- The configurability of an FPGA, the mixed-signal integration of an ASIC, and the familiarity of an MCU.
- Reusable IP, compatible device families and variable resource options so you can optimize design efforts and accommodate changes.
- Two powerful development platforms: PSoC Express™ Software for code-free visual embedded system design and PSoC Designer™ Software for complete flexibility to write code.

GET STARTED WITH PSoC NOW.

- *Download our "Change Happens" White Paper and get 50%* off a PSoC development kit:* **cypress.com/go/changepaper**
- *Download free PSoC Express™ or PSoC Designer™ embedded software:* **cypress.com/go/changesoft**
- *Request free PSoC device samples:* **cypress.com/go/changechip**
- *Free online training:* **cypress.com/go/changetrain**
- *Purchase PSoC development tools:* **cypress.com/go/changetools**



PSoC includes programmable analog and digital blocks, a fast MCU, flash and SRAM memory, all in a compact package (as small as 3mm x 3mm).

CYPRESS PERFORM